SEMICON® Korea 2016

3D and MEMS

Vertical MEMS Probe Technology For Advanced Packaging

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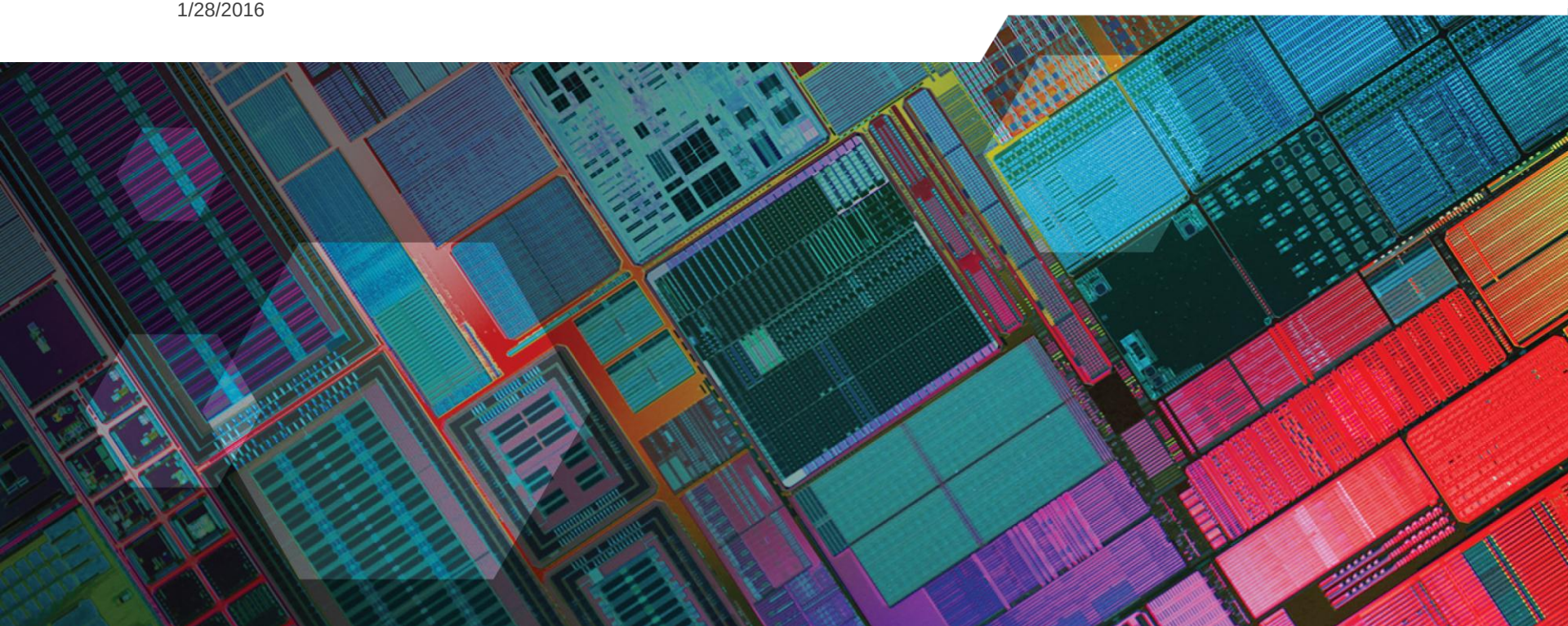
1/28/2016

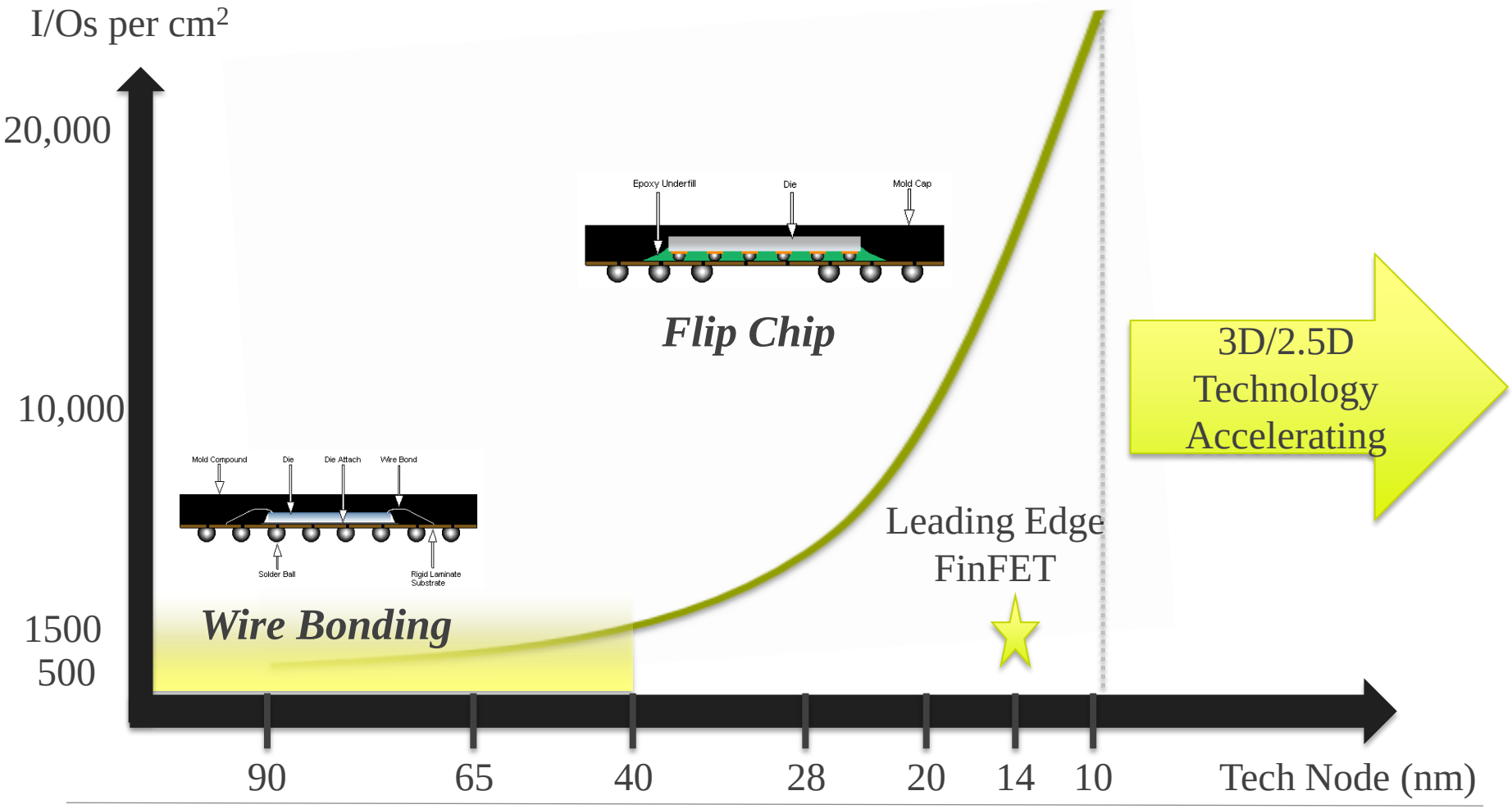


Agenda/Outlines

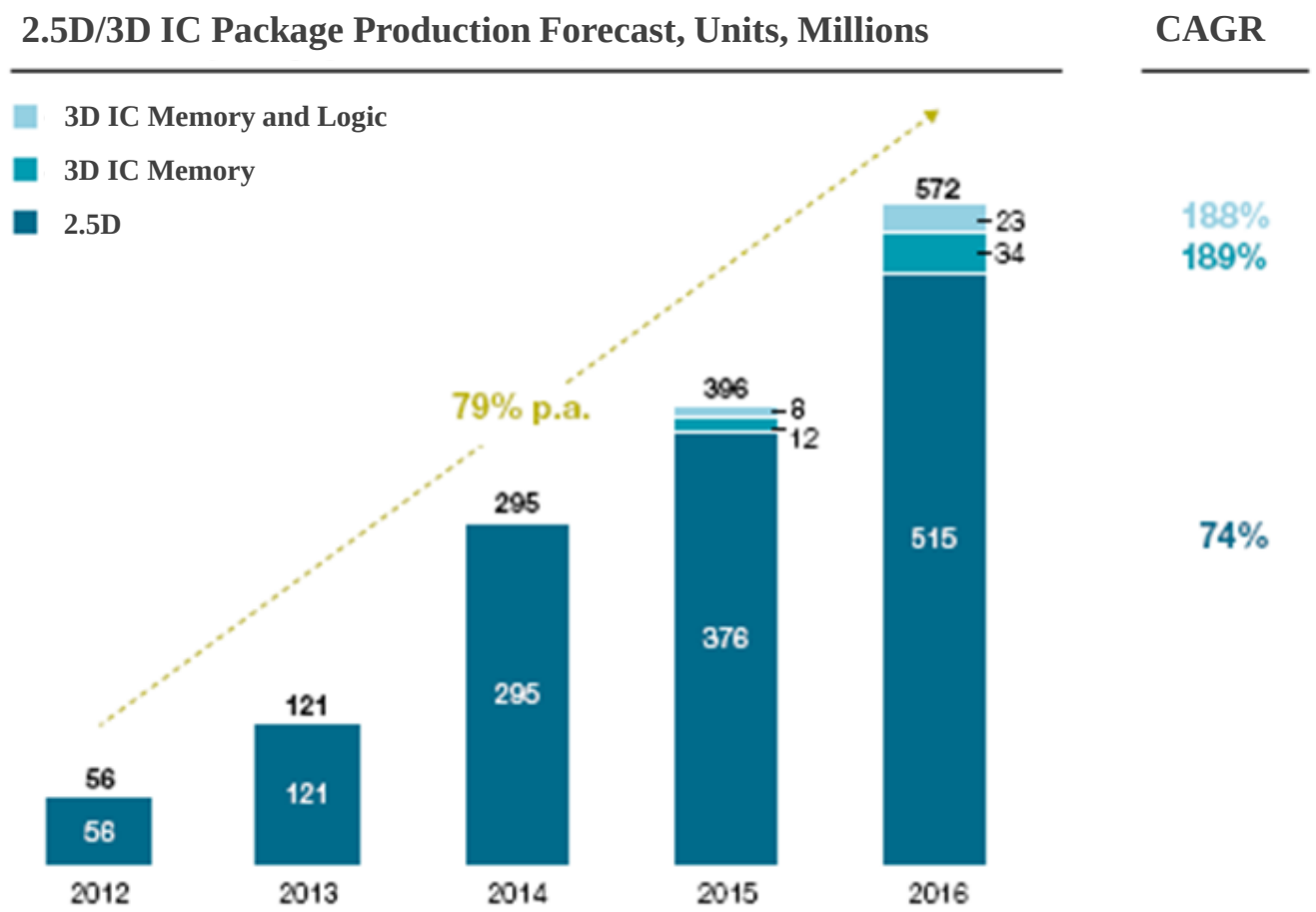
- Rapid recent adoption of advanced packaging
  - Copper pillar and 2.5D/3D ICs
  - Customers relying on “more-than-Moore” advances
- Presents significant challenges for wafer test and probe
  - Layouts are fully-populated 2-D arrays at <100um pitch
  - Contacts are delicate structures made of new and diverse materials
  - Industry requires a “Moore-like” cost and time-to-volume trajectory
- Solutions rely on a synthesis of technologies from diverse areas
  - MEMS processes, materials science, automation, etc.

Transistor Scaling and Cost Reduction Trajectory Slowing

"More-Than-Moore" Advanced Packaging Accelerating Below 10nm



2.5D IC and 3D IC Technologies are growing

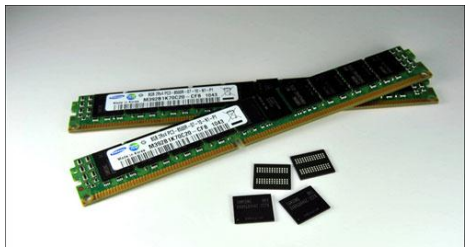


Source: Gartner, New Venture Research, McKinsey

3D IC/2.5D Silicon Interposer Application & Device Drivers

Cu Pillar Enables 3D Fine-pitch Memory Interface and 2.5D Silicon Interposer

- High-end Applications
  - Servers
  - High-end computing
  - Data center
  - Game consoles
- Devices
  - FPGA
  - High-end Memory
    - HBM
    - Wide I/O
    - HMC
  - GPUs
  - CPUs



Samsung DDR4 3D DRAM Module

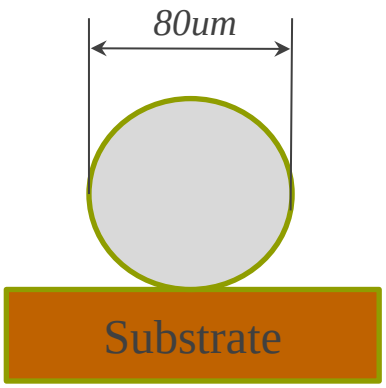
Nvidia Pascal Graphic Module

Intel "Knight Landing" Using HMC

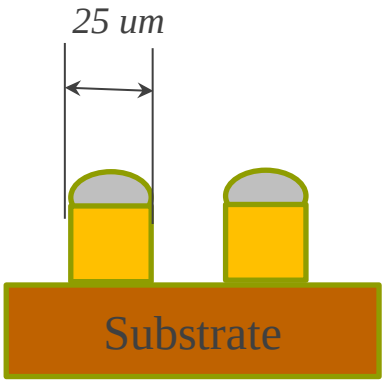
Wafer Probing Challenging

Smaller Cu Pillars at Finer Pitch Require High Contact Precision and Low Force

	Solder Bump	Cu Pillar Dimension Roadmap				
Pitch (um)	150um	130um	100um	80um	60um	40um
Diameter (um)	80 um	60-70um	40-50um	25-30um	20-25um	20-25 um
Height (um)	80 um	75 um	60 um	50 um	40 um	35 um



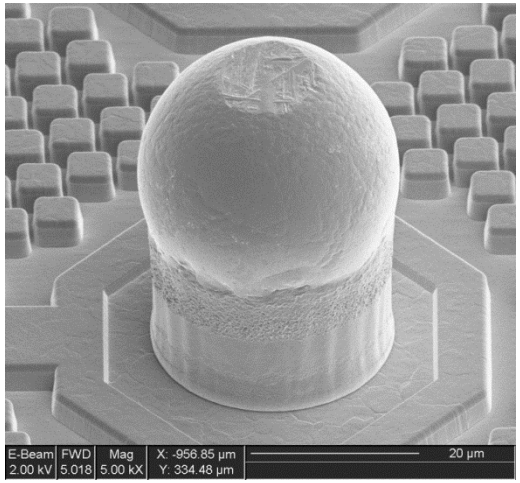
Solder Bump



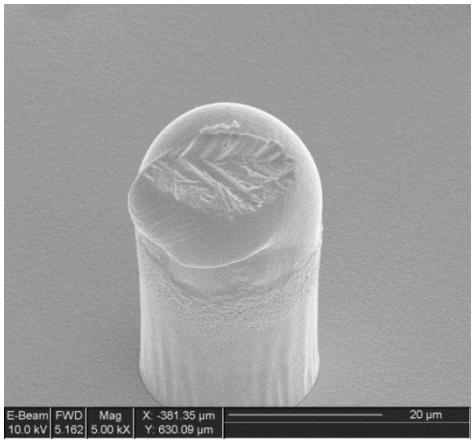
Cu Pillar

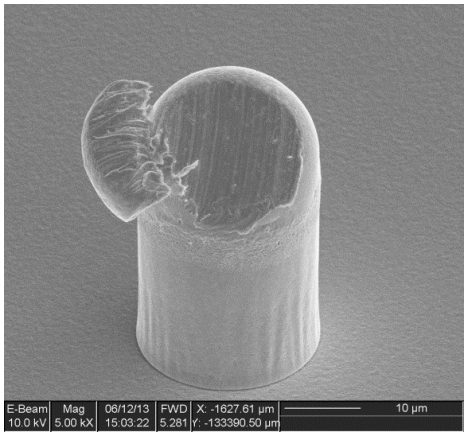
*Source: FFI Estimate, 2015

Cu Pillar Probe Mark Photo Gallery

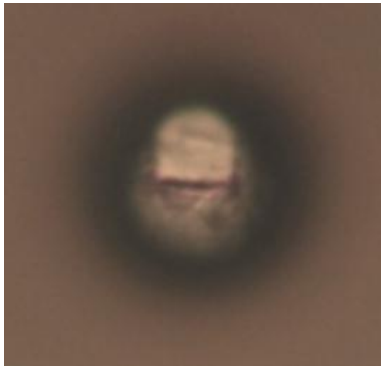


Pass
Good Probe Mark on 30um Cu Pillar

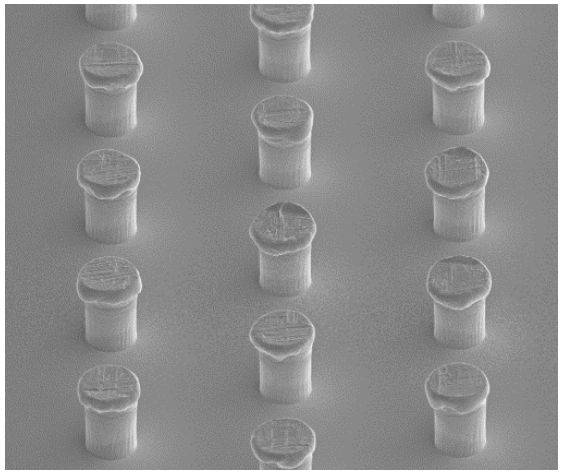




No Pass
Cu Pillars with Sheared Solder Cap



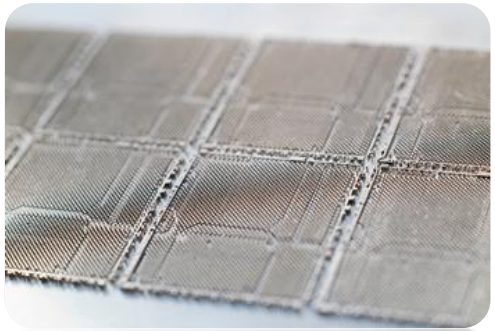
No Pass
Misaligned Probe Tip



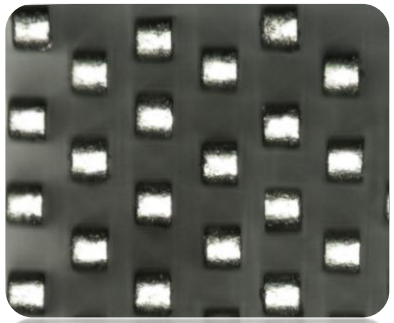
No Pass
Probe force too high

Mechanically Formed Vertical Probes Give Way to MEMs Probes Below 100um Pitch

- Mechanical Tolerances for Stamped probes are inferior to MEMs structures
- Guide Plate Mechanical Drilling is Inferior to MEMs Guide Plate Formation Technology
- Tip Geometries are Poorly Controlled by Stamping and Forming Versus MEMs fabrication
- Contact Materials are Limited to Bulk Alloys for Mechanical Probes but are By Design for MEMs probes.
- Stable Contact at Low Probe Forces is Enabled by MEMs contact Design

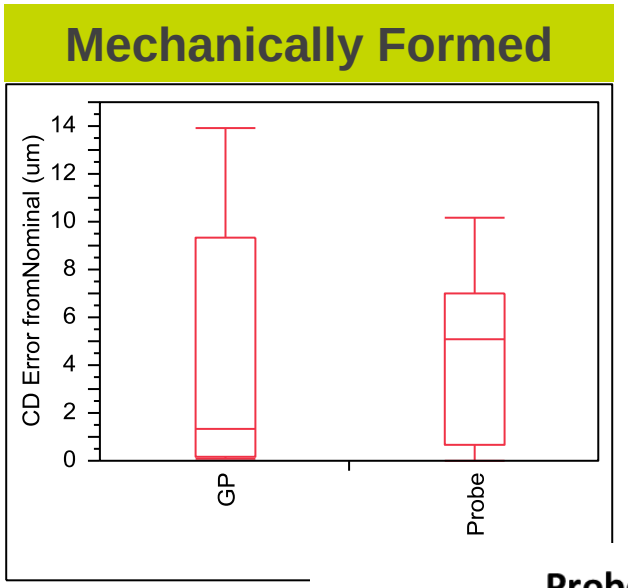


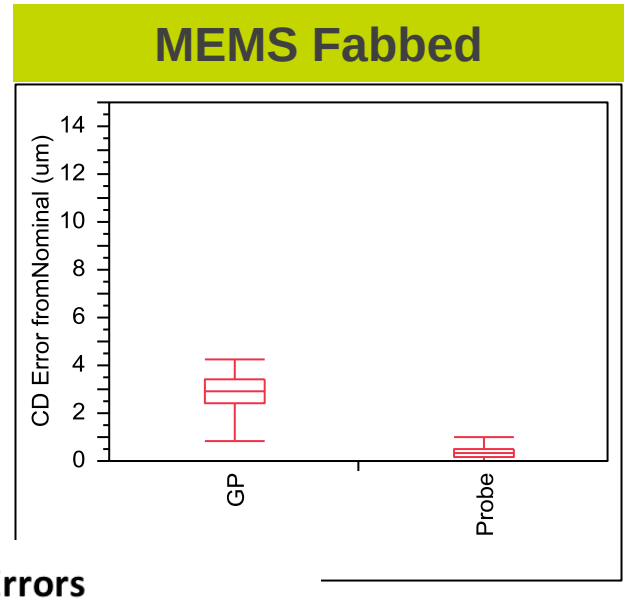
FormFactor
80um Pitch
Grid-array
MEMS Probe



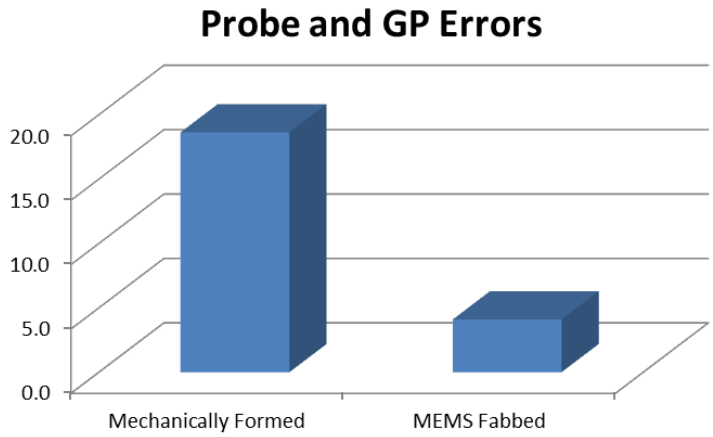
FormFactor
40um Pitch
Grid-array
MEMS Probe

Dimensional Control Improved With MEMS-Based Fabrication Processes

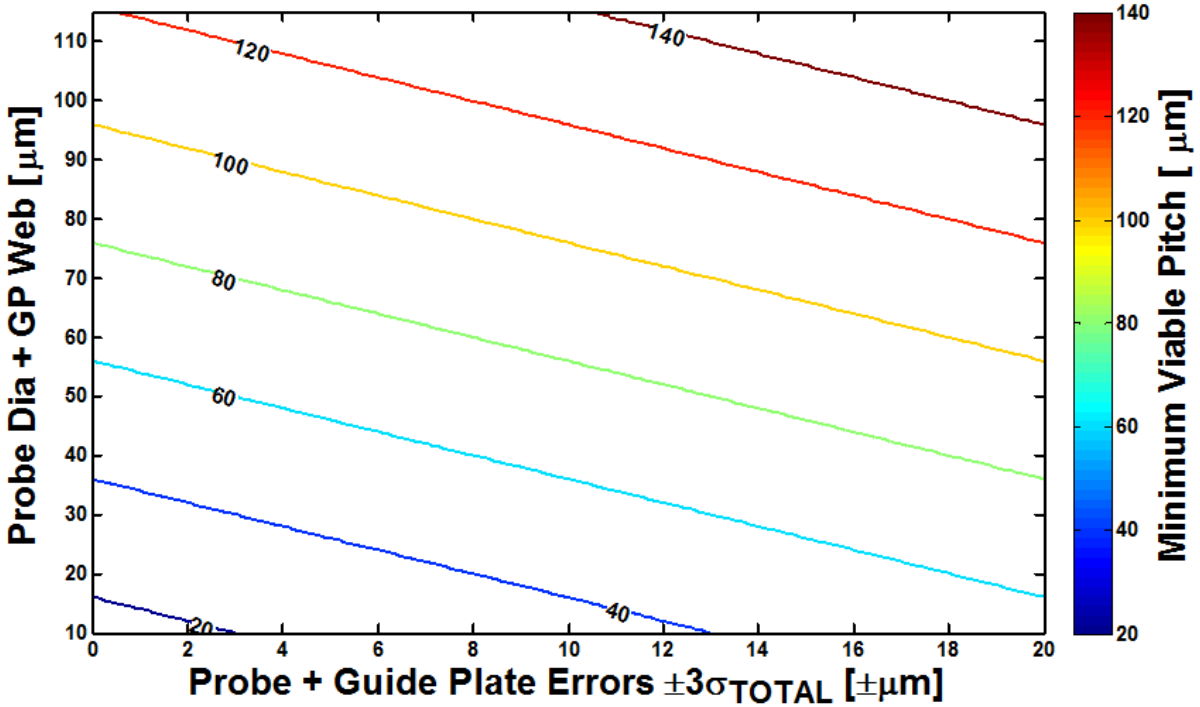




- Raw "as-fabbed" distributions
- Indicative of natural process capability



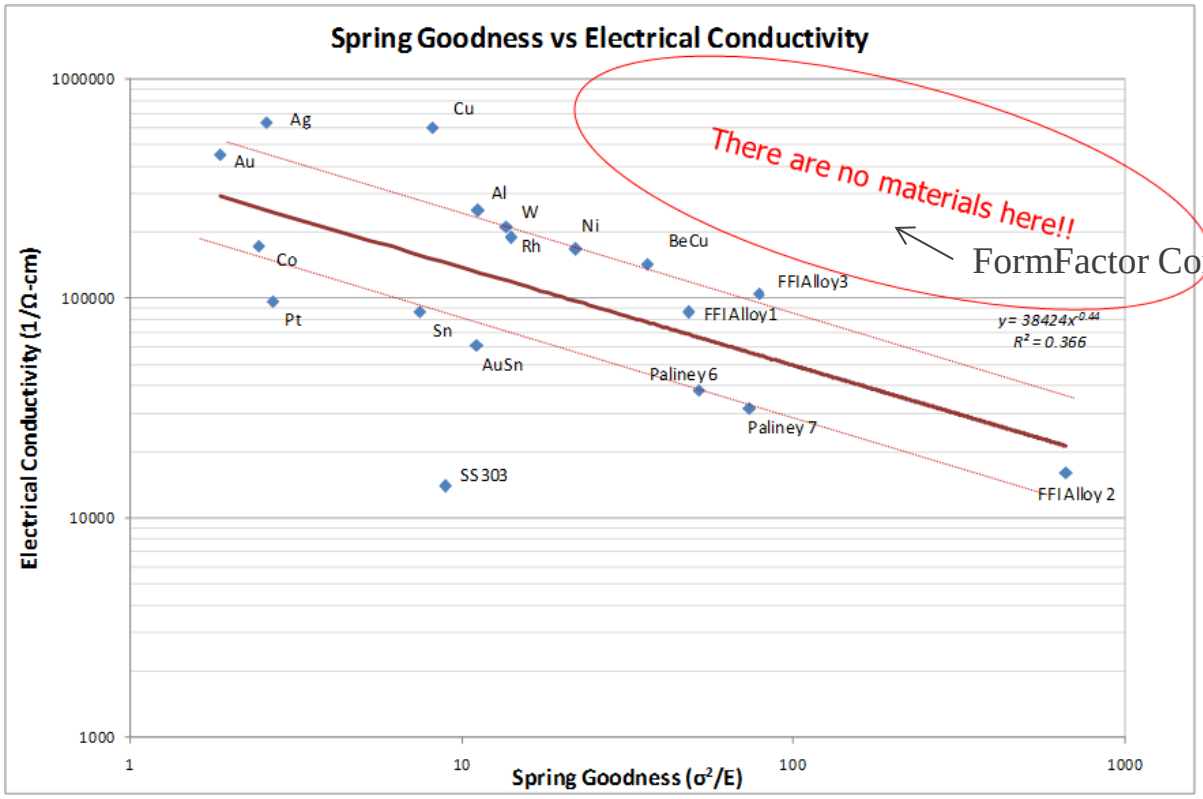
For Sub-100um Pitches, MEMS-based Dimensional Control Offers Significant Advantages



Reduction in as-produced dimensional errors can be used in different ways

- Larger probe for a given design pitch - for 80um example above, Δ=25um
  - Better electrical performance (current, impedance) and longer lifetime
- Smaller minimum-viable pitch for a given probe
  - Improved design coverage and extendibility
- Higher probe/GP component yield for cost reduction

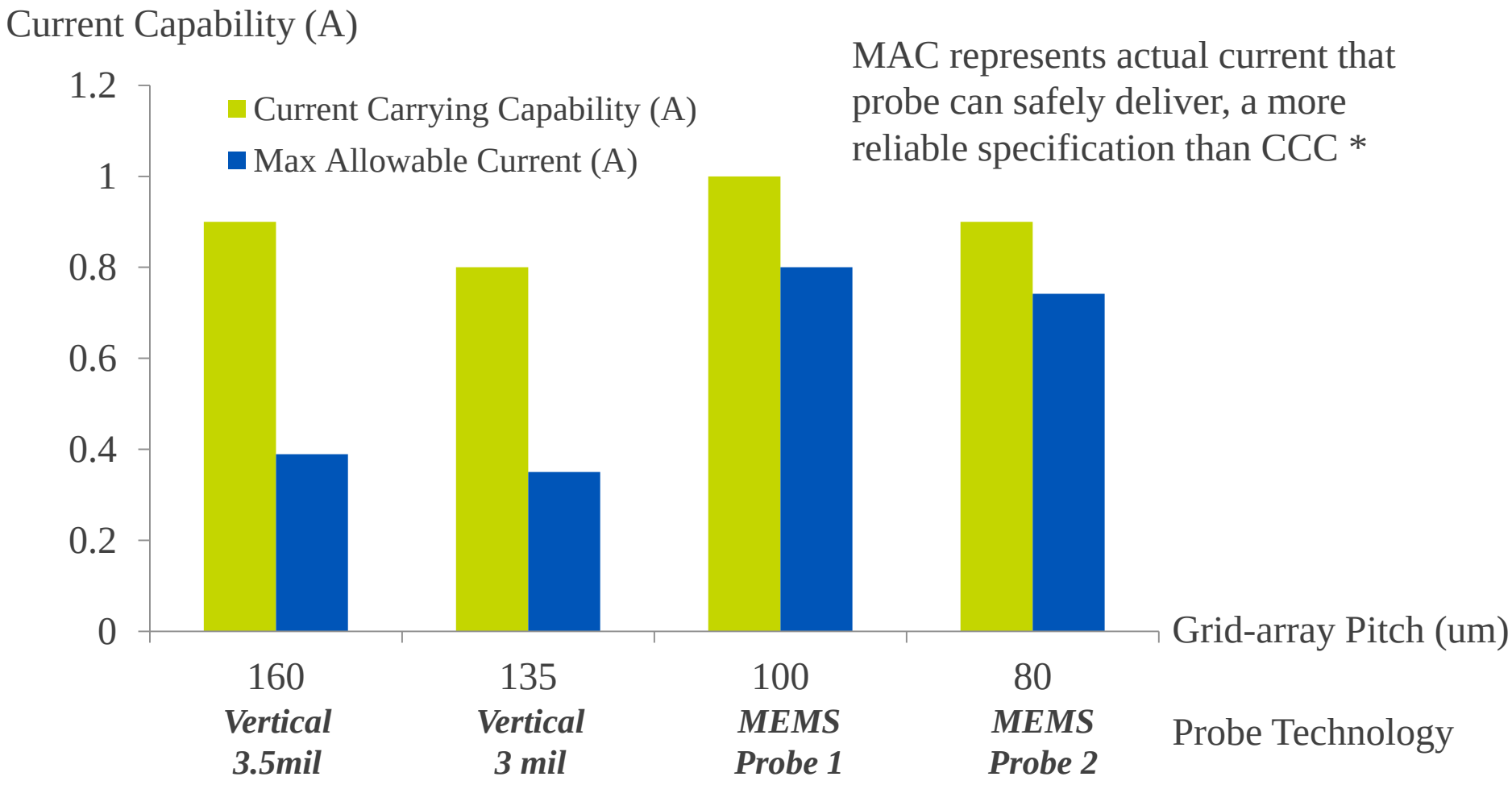
Composite MEMS Structure Helps to Carry More Current Through An Ever-Shrinking Probe Cross-Section



- Geometries are getting smaller, while current densities are increasing
- Composite MEMS probes made from different material
  - Analogous approach to composite design in other fields (eg, aerospace)
  - Broad material set for best mechanical **and** electrical performance

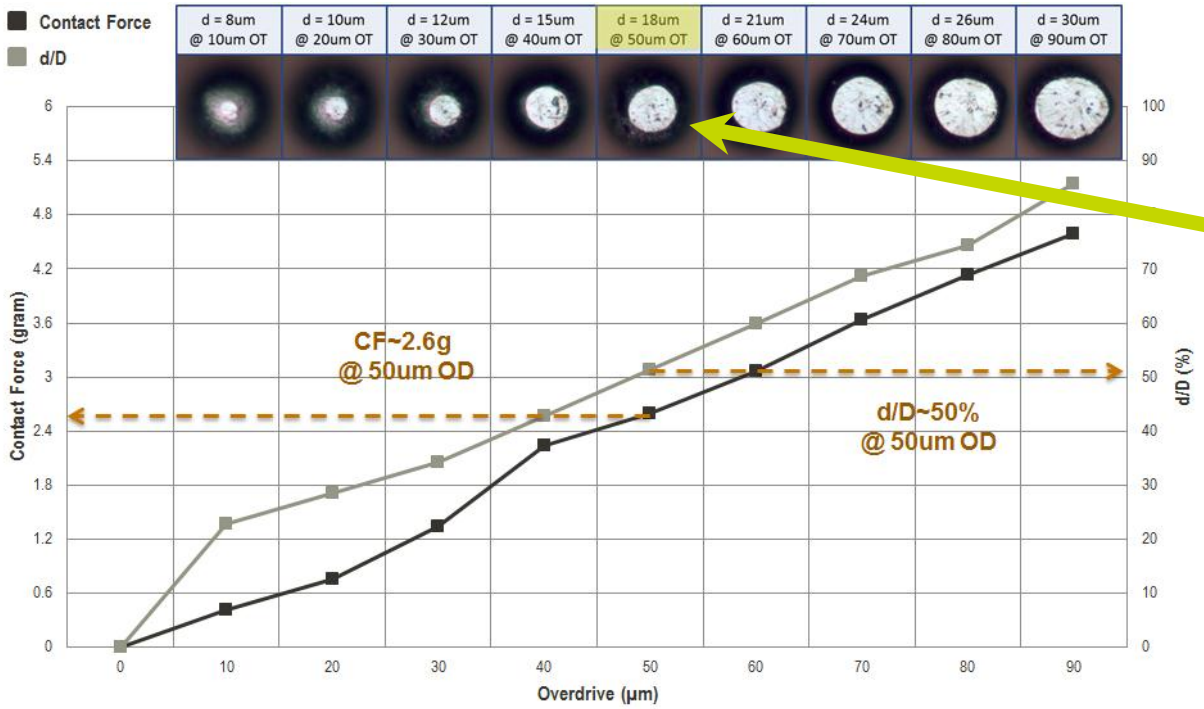
Maximum Allowable Current (MAC) vs Current Carrying Capability (CCC)

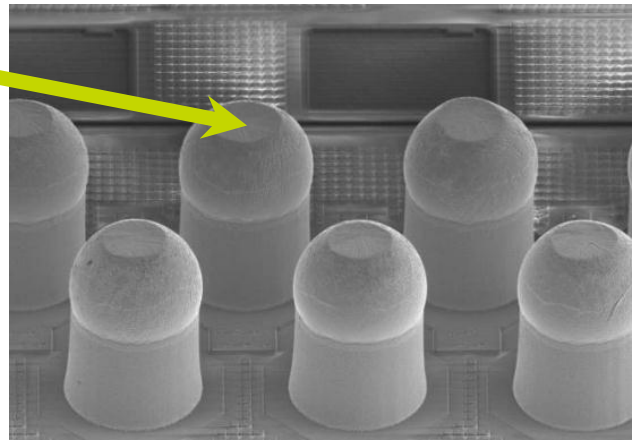
MAC to CCC Ratio is not constant, is probe architecture dependent*



Source: "Determining Probe's Maximum Allowable Current", Kister et al, SWTW 2015

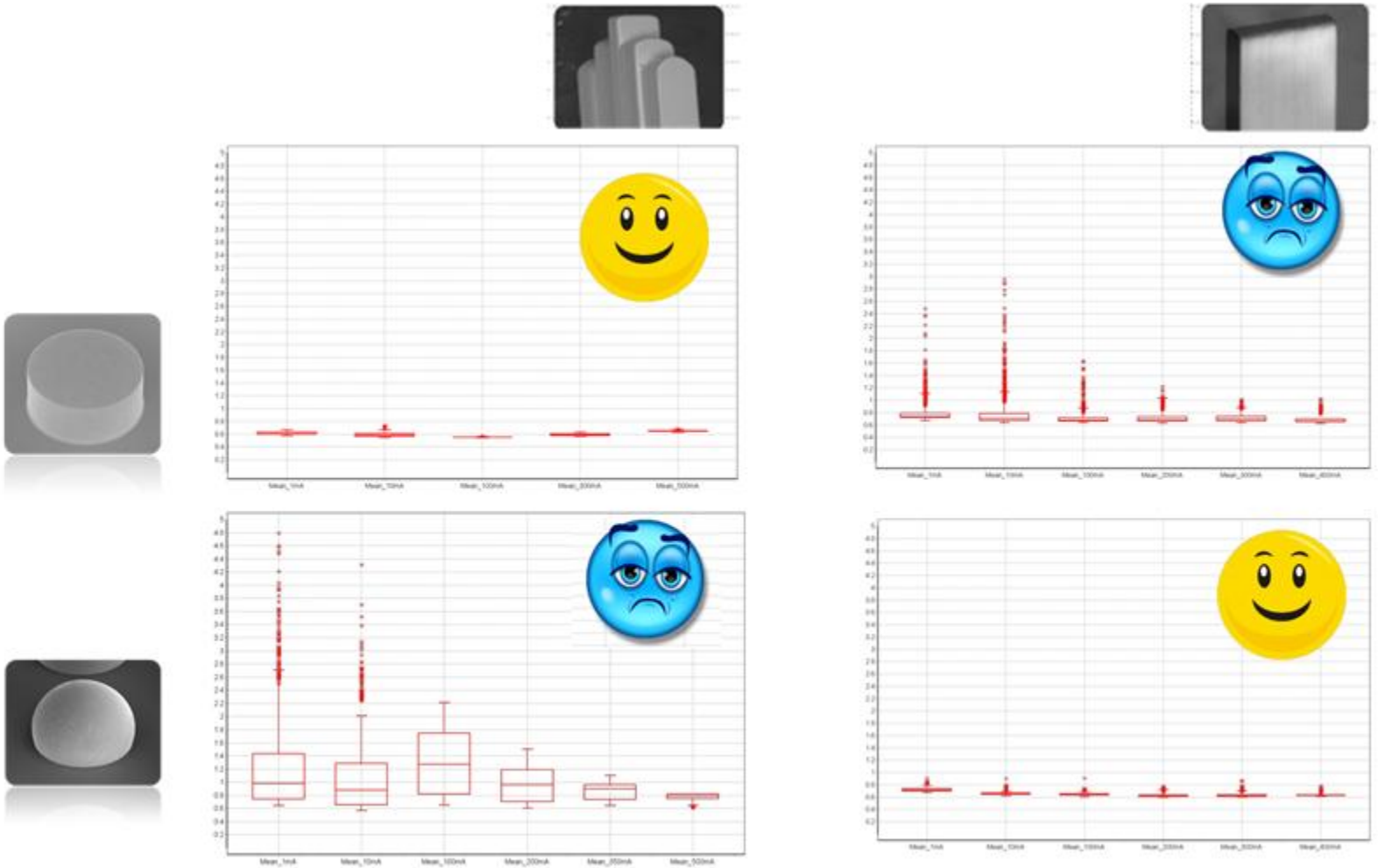
These 2-D Layouts are Populated With Structures That Require Low Probe Forces





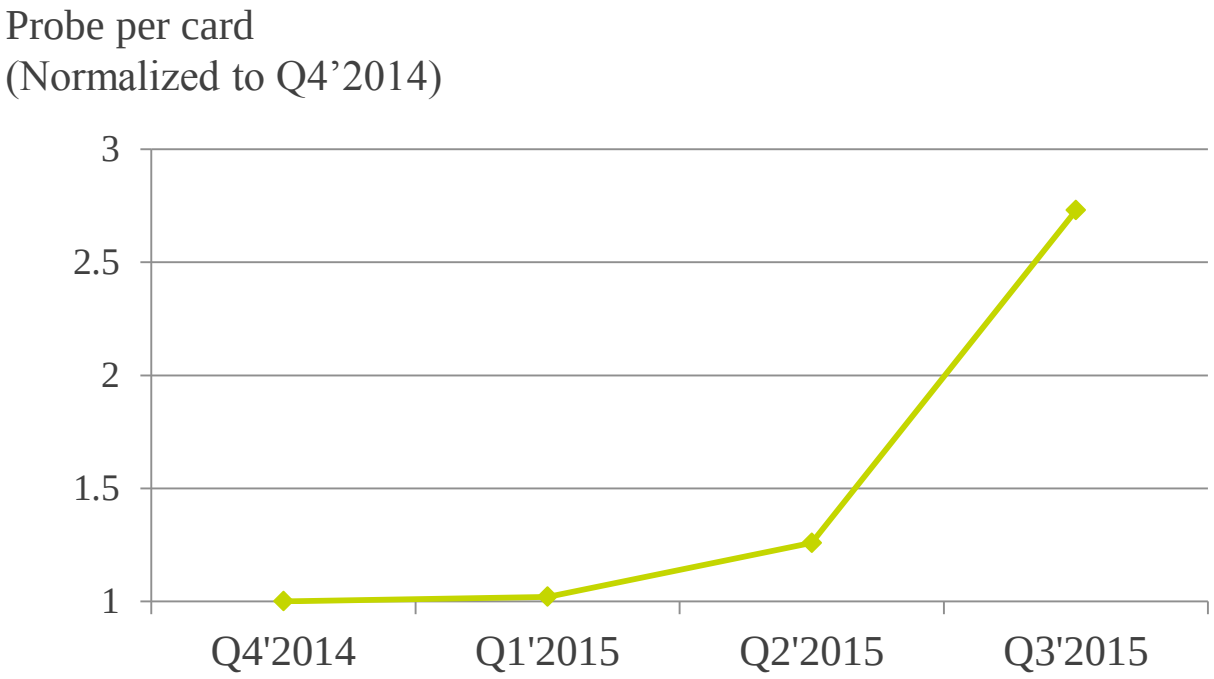
- Typical SnAg damage (d) requirement <50% of pillar diameter (D)
  - Additional requirements on probe mark topology (notching, smearing, etc.)
  - Imposed by assembly constraints (reliability)
  - Met with probe forces of <2-3g for 30um < D < 40um

At Low Force, Probe Material and Geometry Optimization Required for Stable Electrical Contact



Source: Data from Wittig et al, SWTW 2011

There are More and More of These Probes in Each Card

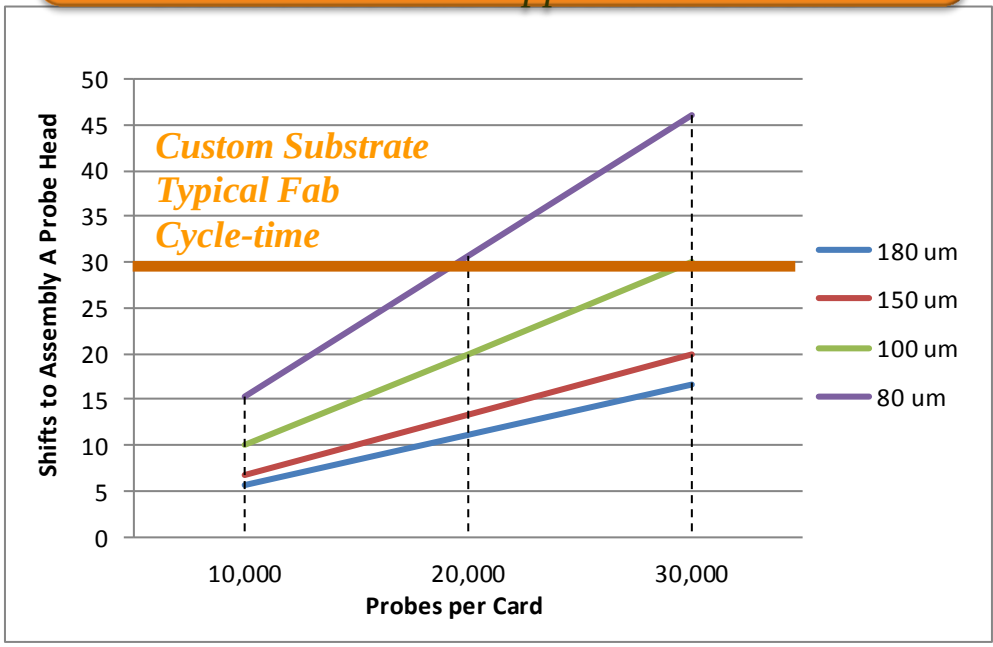


- Two primary drivers/causes (roughly equal influences)
  1. Increased parallelism – more DUTs for test cost reduction
  2. Increased probes per DUT – more test content and complexity per DUT

Probe Assembly Throughput Is Becoming An Issue for Probe Card Cycle-time @ 80um CuP Pitch

Vertical Probe Assembly Throughput Decreases with Slimmer Probes

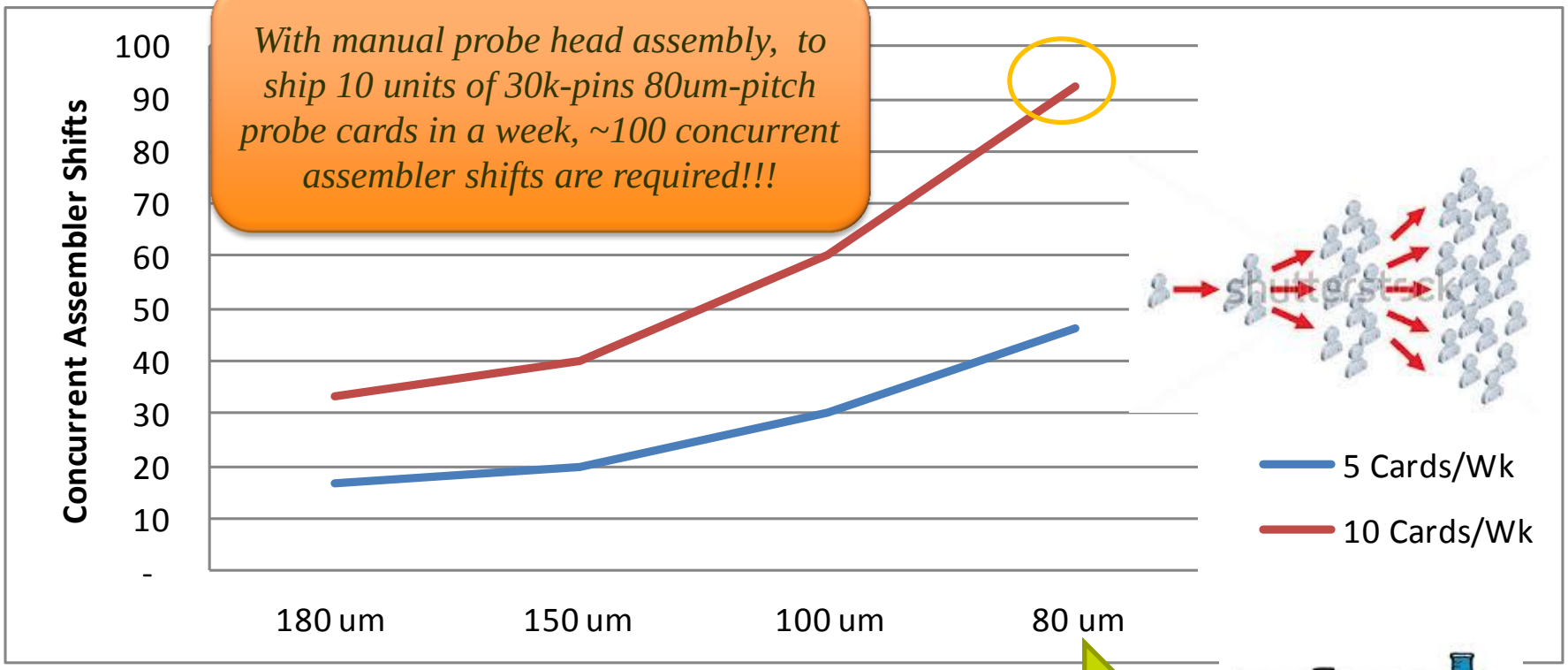
Probe Head Assembly Is Becoming the Critical Path to Probe Card Cycle-time As Pin Counts/Probe Card Approaches 20k Pins

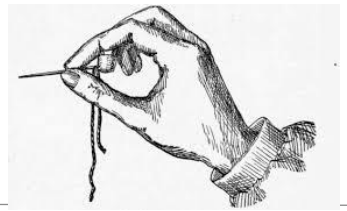


Time-to-Volume Ramp-up @ 80um CuP Pitch

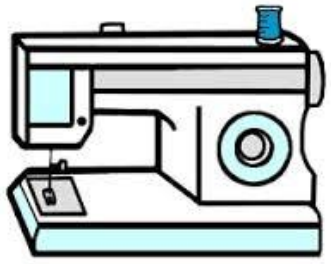
What if 5 or 10 cards are needed in a week to address peak demand?

With manual probe head assembly, to ship 10 units of 30k-pins 80um-pitch probe cards in a week, ~100 concurrent assembler shifts are required!!!





"Hand to Machine" Conversion Begins @ 80um Grid-array CuP Pitch



Summary

- Static trend of grid-array packaging pitch is turning into rapid reduction
  - 150um -> 130um -> 100 -> 80um -> sub-50um
- Grid-array assembly pitch roadmap is converging with 2.5/3D TSV Cu Pillars
  - pitch, bump geometry, bump material sets
- Conventional technology can't keep up with the current trend
  - Low-force, Alignment, Current Carrying Capability, Assembly Method
- MEMS probe contact technology is required to keep up with the increase in packaging I/O density and decrease in pitch
- FormFactor is developing multiple contactor technology to address the probe/test challenges for 2.5D/3D structures
- A complete Contact technology Roadmap for Cu Pillar uBumps and Silicon Interposer probing