



IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Use of Resource Sharing Techniques to Increase Parallel Test and Test Coverage in Wafer Test



FORMFACTOR



MICROPROBE™

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Motivation

- **With increasing test times/DUT and die per wafer, test time/wafer and test cost were increasing**
 - Increase of parallel test was identified as the solution to get out of this dilemma
 - Impact on test coverage, yield needed to be minimized
- **DFT and TRE were developed to enable higher parallel test**

Trend in Parallel Test of DRAM

Tester Sites	16	32	64	96	64	96	96/128
Parallelism	16	64	256	384	512	768	~1000
Signal TRE	x1	x2	x4	x4/x6	x8	x6/x12	x8/x16
DFT	No	I/O compr.	I/O compr.	I/O compr.	I/O and control	I/O and control	I/O and control
A-TRE	none	none	none	none	DC-TRE PPS-TRE	DC-TRE PPS-TRE	DC-TRE PPS-TRE

- Which other capability will be needed in the future to get to the next step?
- Test time impact is very much in focus

Michael Huebner
“High Speed Control Bus for
Advanced TRE”
SWTest 2010



Introduction

- **Test Resource Enhancement = TRE**
 - Sharing of tester resources between multiple DUTs using passive components.
- **Advanced TRE**
 - Sharing of test resources using active components and having the ability to connect and disconnect DUTs from the tester resources
 - Other active circuits to increase tester capabilities
 - Current, Frequency ...



Signal TRE - Principle

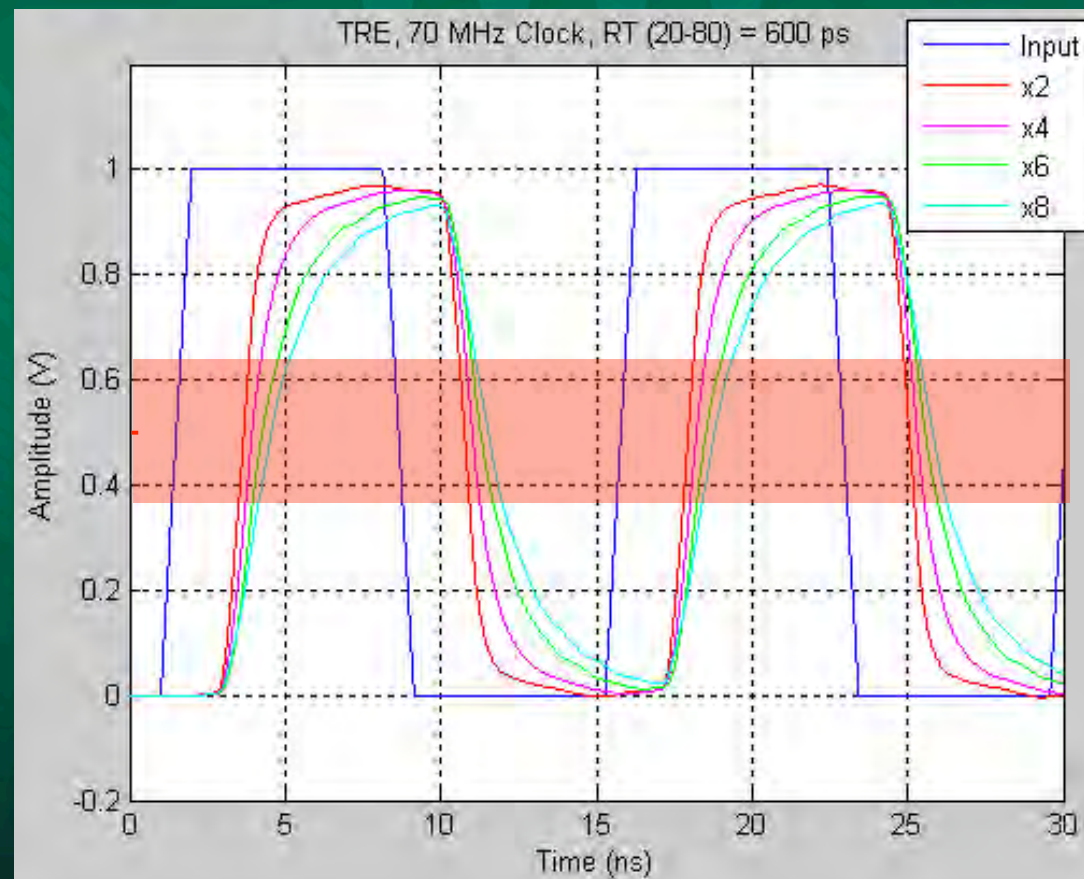
- **Tester driver resources are used on multiple DUTs at the same time**
 - Typical signals: CLK, address, other controls (WE, CS..)
 - Tradeoffs: Signal integrity and “dead soldier” impact
 - Optimize sharing pattern to avoid sharing over the wafer edge
 - With and without resistive protection (OhmGuard™)

X4 Shared Control



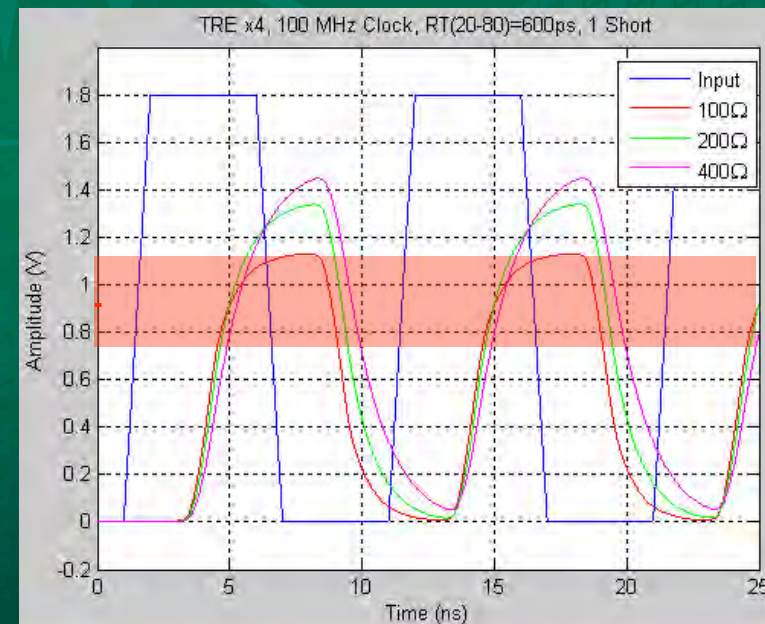
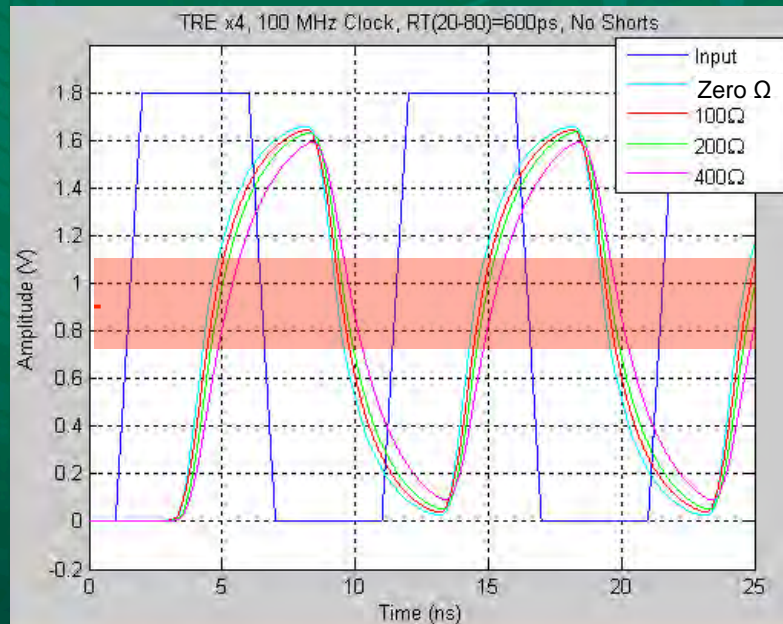
Signal TRE – Things to consider

- TRE impacts the signal integrity (rise time, etc.)
 - Decreasing rise time with higher sharing factor



Signal TRE – Things to consider

- **Dead soldiers are impacting signal waveform**
 - Critical: Isolation resistor value and number of shorts
 - Which signal level is required?



Signal TRE – Things to consider

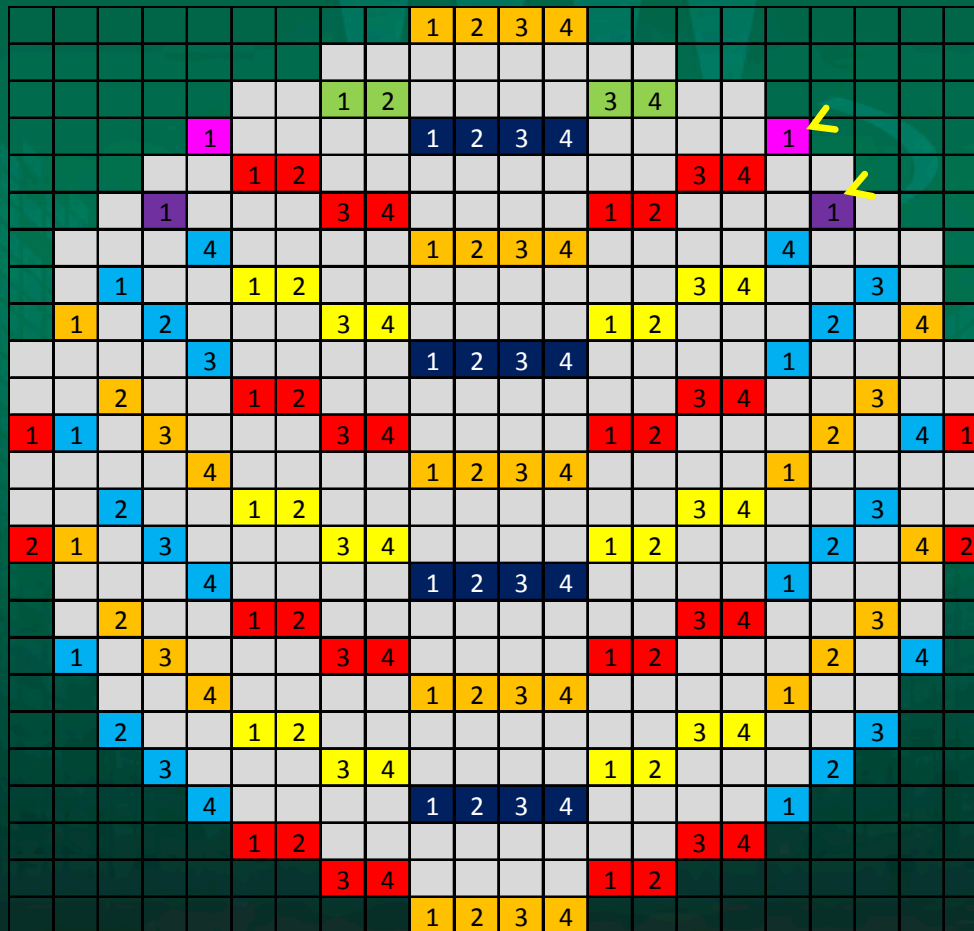
- **Strategies to minimize dead soldier yield loss:**
 - Adjust TRE/sharing pattern to wafer map to reduce potential yield loss by e.g.:
 - Minimize sharing across the wafer edge by smart layout of the sharing pattern
 - All DUTs of one shared group should be either completely on the wafer or all off the wafer during one touchdown
 - Combine DUTs which step off the wafer in same step in one group
 - Highest sharing inside the wafer – reduced sharing at the wafer edge – if resources are available



Signal TRE – Things to consider

- Example for design of shared groups minimize sharing across the wafer edge

Stepping direction
3 TDs

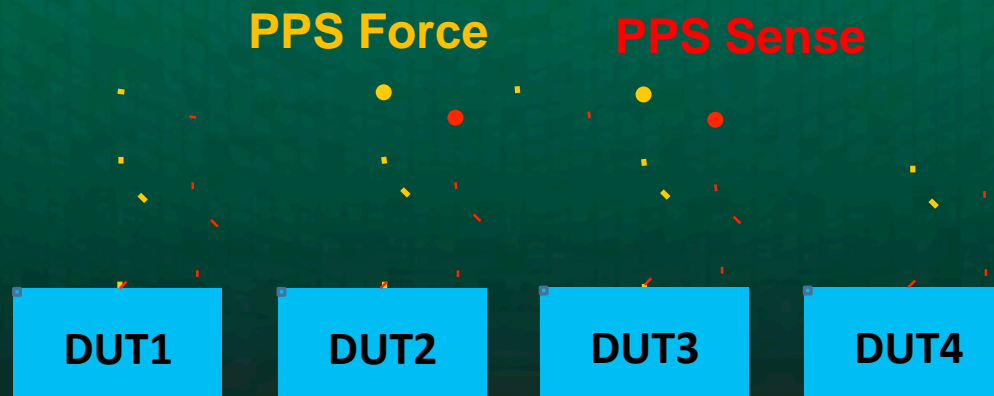


- Step out on 2nd TD
- Step out on 3rd TD



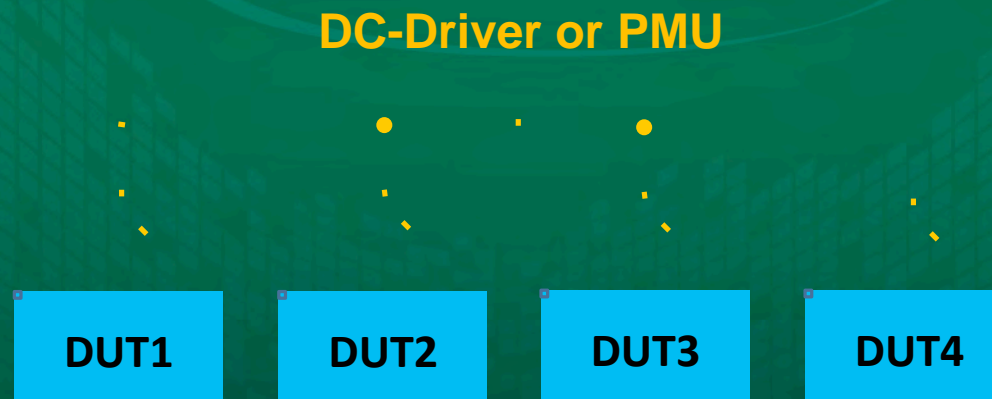
A-TRE: Power Supplies

- **Power Supply sharing requires switches to connect and disconnect DUTs from tester power supply**
 - Disconnect DUTs during current measurements
 - Disconnect bad DUTs with high current from shared group
 - Max sharing is limited by current capability of power supply and consumption of DUT
 - Separated switches for Force and Sense are used in case of low power devices to minimize voltage drop (as shown below)



A-TRE: DC-Signals

- Sharing of DC-resources requires switches to disconnect DUTs from tester DC-resource
 - X-DUT DC-TRE
 - IN-DUT DC-TRE



x4 X-DUT DC-TRE



A-TRE: DC-Signals

- **X-DUT DC-TRE**

- Forcing of voltage to DC-pads on the DUT
 - All switches closed
 - Individual switch control is required for disconnection of bad DUTs which would pull down signal level
- Voltage/current tests or chip individual voltage trimming
 - Only one chip is connected at the same time
 - Sequence control is sufficient in this case
- Different signals can be forced or measured at the same time

DC-Driver or PMU



DUT1

DUT2

DUT3

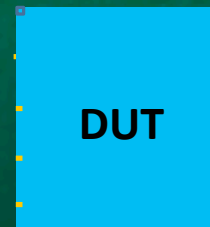
DUT4

A-TRE: DC-Signals

- **IN-DUT DC-TRE**

- One DC-resource is connected to multiple DC-signals on the same DUT
- Sequential control is sufficient – no need for individual DUT control
 - Easy to implement and to control
- Less flexible in terms of test capability – Force or measure only one signal at the same time

**DC-Driver
or PMU**



A-TRE: AC-Signals

- **TRE on AC signal is enabled through AC-switches**
 - Perfect isolation – better than resistive isolation
 - Share control lines between different signals on one DUT
 - Pull-up/down of signals

HF Driver



DUT1

DUT2

DUT3

DUT4

DUT

HF Driver

DUT



HF Driver

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A-TRE: I/O-Signals

- **AC switches on I/O channels can be used to increase parallel test without on-chip I/O compression**
 - Parallel Write and Sequential Read controlled by switches
 - Used for Flash testing where Write takes longer than Read, overall test time benefit can be achieved
 - Also used for WLBI when individual Read back is not required in every stress cycle



Typical Application: DRAM

- **Typical DRAM test scenario**

- Signal TRE x4/x6/x8 or higher
- I/O compression
- DC-TRE
- PPS-TRE

X6 Shared
Controls 10-15

I/O 2

DUT1

DUT2

DUT3

DUT4

DUT5

DUT6

Power-TRE
switches

DC-TRE
switches

Power-TRE
switches

DC-TRE
switches

Power-TRE
switches



Design For Test/DFT

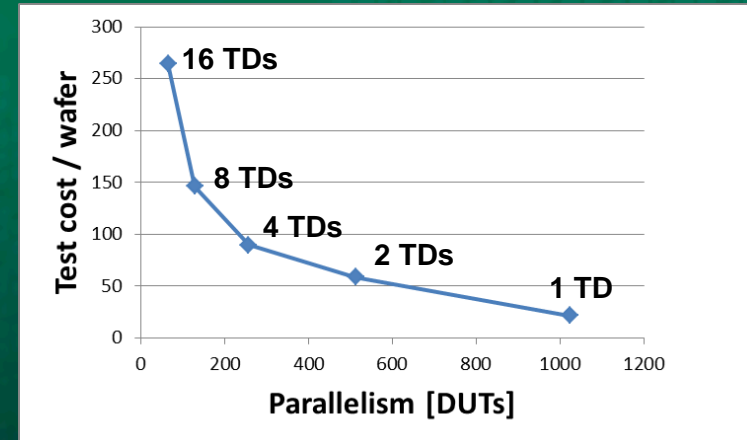
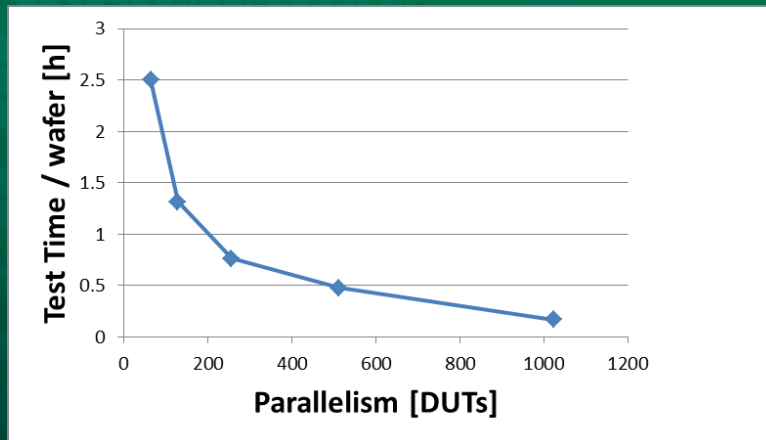
- **DFT and TRE were developed to increase parallel test**
- **DFT- examples:**
 - I/O compression: 4 or 2 or 1 I/O mode (out of 16 I/Os)
 - Address compression test modes to reduce the number of driver channels needed to control the DUT
 - Internal DC-signal MUX to reduce number of tester resources needed
- **Tradeoffs: Die area, yield, test time impact, time to market**



Typical Application: DRAM

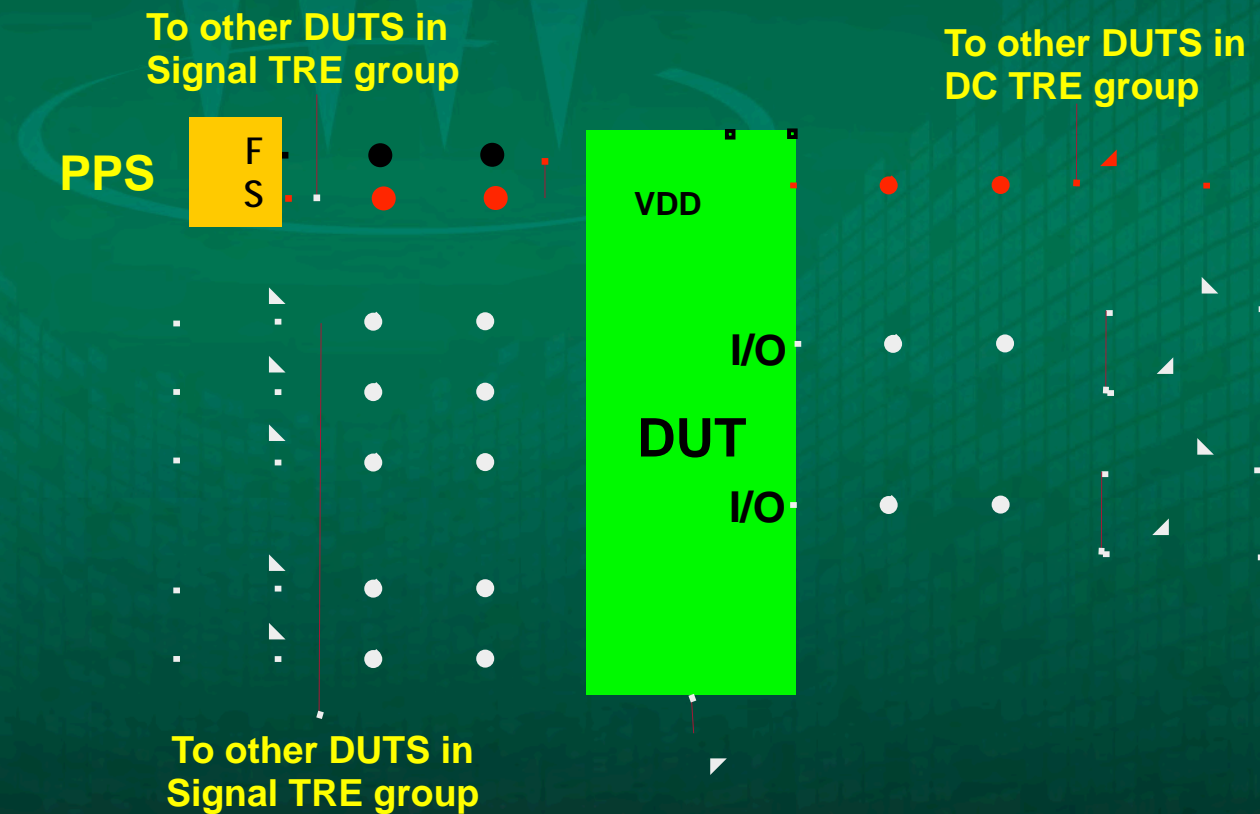
- **Benefits of parallel test**

- Test time and test cost per wafer are reduced dramatically
- Scenario below shows change from 64DUT to 1024 DUT on most commonly used DRAM testers
- Test time overhead and higher probe card price are considered as well



Typical Application: Flash

- **Total isolation: All signals can be disconnected**
 - I/O and data signals
 - DC-signals
 - Power



A-TRE for SOC

- **Run for high parallel test just starting - may not be possible for all applications due to tester limitations**
 - Easier for Memory like test problems like Embedded Memory on SOC
- **Technology developed for DRAM/Flash can be used for**
 - Increase of parallel test
 - Increase of test coverage in case there is a lack of certain resources (or current?)
 - New test features can be implemented on old testers extending the useful life of test systems



Need More Current?

- Voltages level are going down – current is going up
- Tester power supplies provide max current at max voltage: e.g. 0.8A @ 5V
 - Typical voltages are 1.5V and below
- Use DC/DC converters to create higher current at lower voltage
 - Using PPS-TRE switches to distribute new more capable power supply channels (with current trip function?)



A-TRE Components

- **Requirements:**

- Size matters – highest integration needed
- High temperature up to 125°C
- Serial control for complex control schemes
- Low current demand

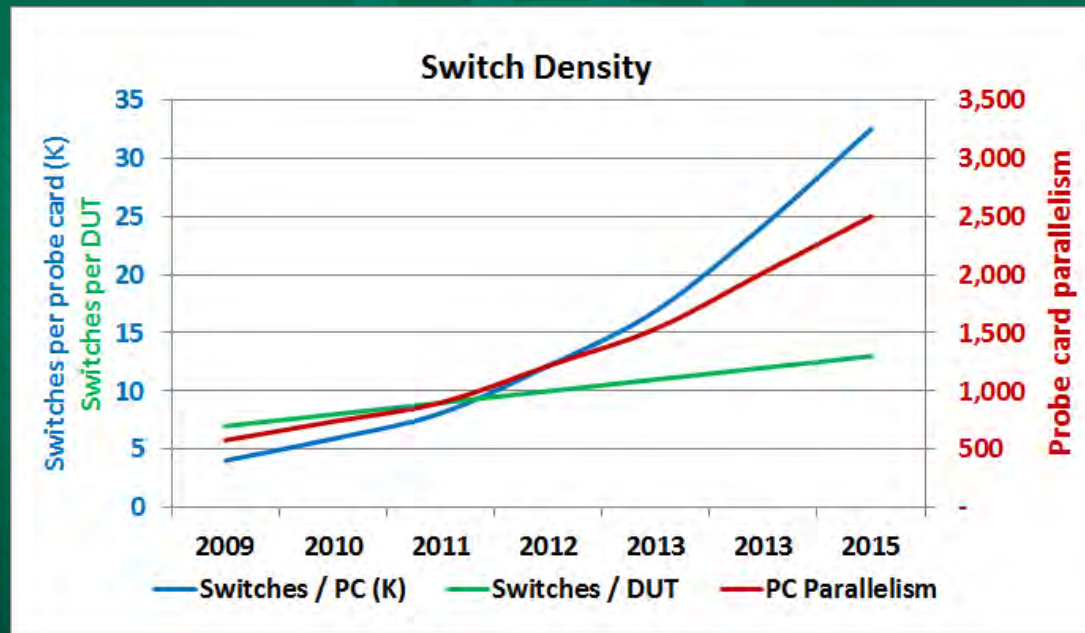
- **Typical components used:**

- FETs and analog switches
- PhotoMOS – limited by size and current
- Custom ASICs – switches with serial control
- Controller: CPLDs, FPGAs, Microcontroller



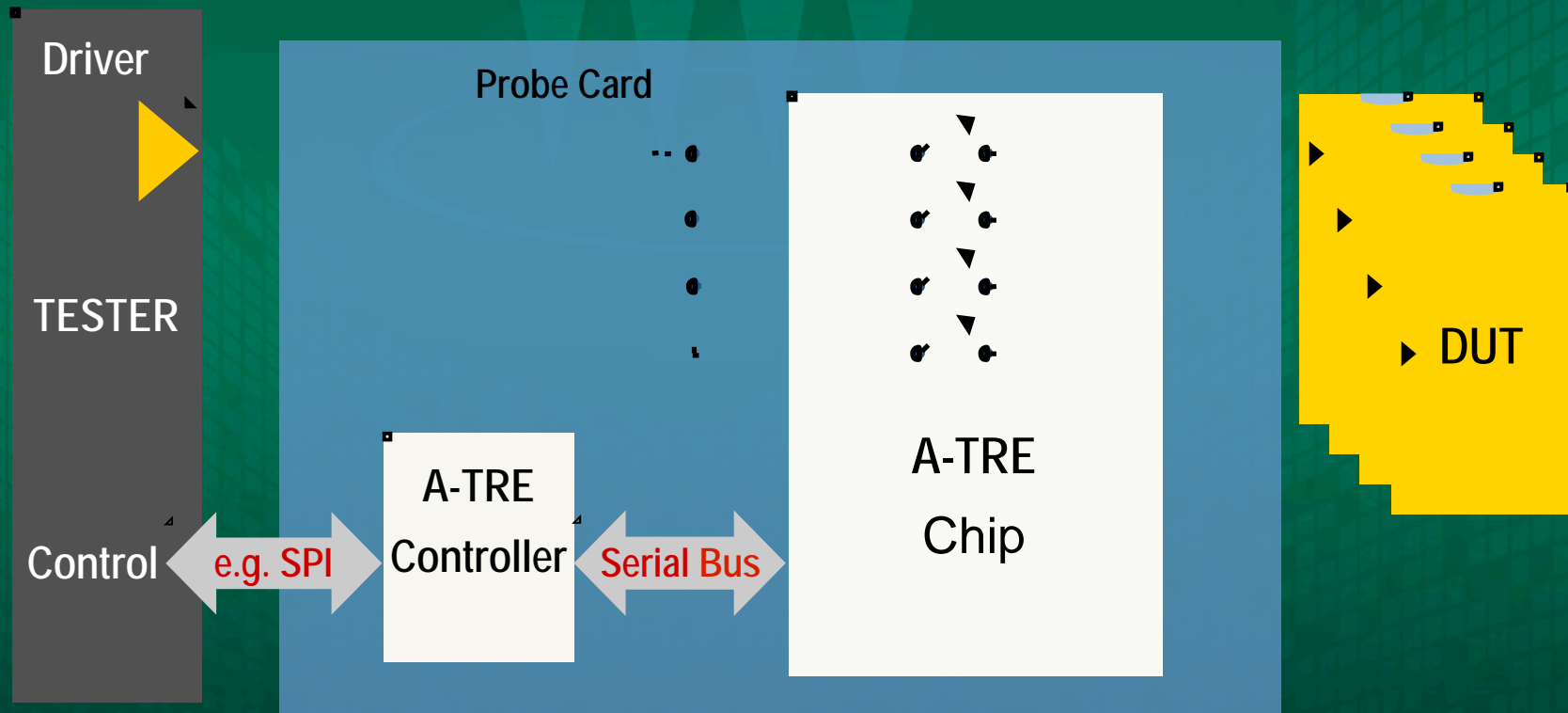
Roy's Law

The number of switches on a probe card doubles every second year.



How to control A-TRE?

- Example of A-TRE control using SPI bus from tester and serial bus on probe card



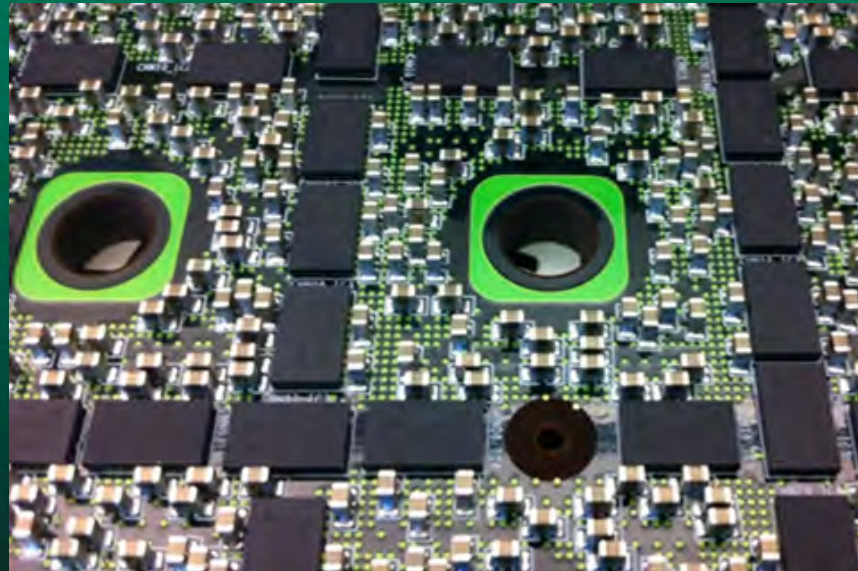
Guiding Principle of TRE

- **Start with your testing problem**
 - How many resources are needed for the given device and test needed to be performed?
 - How many tester resources with the required capability are available?
- **In case there is a shortage of resources or capability what can be done to overcome this shortage?**
- **On the probe card you have the flexibility to boost your tester performance and overcome its limitations**



Achievements

- **Typical high end cards for DRAM**
 - 1000 DUTs
 - 2 power switches and 2 sense switches per DUT
 - 4 DC-TRE switches
 - Total of 8000 switches and 4000 capacitors
 - Very high component density



Summary

- **TRE and Advanced TRE have been developed to extend test capability for higher parallel test and increasing test coverage**
- **Today high volume production test of most DRAM and NAND Flash is using a combination of TRE, A-TRE and DFT**
- **Other application can also profit from using the methods developed**
- **Many things are possible on a probe card to respond to changing device test requirements.**



Acknowledgements

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 - Nick Sporck
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