Register today for COMPASS 2014, Cascade Microtech’s second annual users’ conference, scheduled at the end of European Microwave Week in Rome, Italy. COMPASS 2014 offers a great lineup of speakers – our industry leaders and subject experts will be sharing their perspectives on meeting the emerging test challenges with innovative and practical ideas. COMPASS 2014 also provides excellent networking opportunities with test and measurement peers, as well as Cascade Microtech’s management and technical experts and solution partners.

Don’t miss COMPASS 2014!

**Keynote: The New IC — Innovation and Collaboration — and its Impact on Test**

**John Y. Chen** Vice President of Technology & Foundry Management, NVIDIA

Dr. Chen has been in the semiconductor industry for over 36 years and has served as the Vice President of Technology and Foundry Operations at NVIDIA Corporation, the world leader in visual computing technologies, for over ten years. Prior to joining NVIDIA, Dr. Chen, an IEEE Fellow, held senior executive positions at FlexICs, Inc., Taiwan Semiconductor Manufacturing Company, WaferTech LLC, and Cypress Semiconductor Corporation.

At COMPASS 2014, he will review recent market trends driven by the exploding Cloud, mobile and “Internet of Things” and discuss his perspectives on the challenges of meeting manufacturing and testing needs, while increasing efficiency and reducing overall costs.

**Featured Session: The 5G Communication System - A Holistic view**

Frank Fitzek, Professor and Chair of Communication Networks at the Technische Universität Dresden, will reveal a holistic view of 5G communication systems of the Dresden 5G Lab, review 5G use cases and the derived technical challenges, and introduce the key technologies supporting the technical challenges.

Since 2014, Prof. Fitzek has been leading the Communication Networks at the Technishe Universität Dresden. His current research interests are in the areas of wireless and mobile communication networks, mobile phone programming, network coding and cross layer, as well as energy efficient protocol design and cooperative networking.
Session Descriptions

**TRACK 1: FINE-PITCH PROBING**

**Direct Probing on Large-Array Fine-Pitch Micro-Bumps of a Wide-I/O Logic-Memory Interface**
Presenter: Ken Smith, Cascade Microtech (Co-Authors: Erik Jan Marinissen and Bart De Wachter, imec, Mottaqiallah and Said Hamdioui, Delft University of Technology, and Jorg Kiesewetter, Cascade Microtech)

In order to obtain acceptable compound stack yields for 2.5D- and 3D-SICs, there is a need to test the constituting dies before stacking. The non-bottom dies of these stacks have their functional access exclusively through large arrays of fine-pitch micro-bumps, which are too dense for conventional probe technology. A common approach to obtain pre-bond test access is to equip these dies with dedicated pre-bond probe pads, which comes with drawbacks such as increased silicon area, test application time, and reduced interconnect performance. In order to avoid the many drawbacks of dedicated pre-bond probe pads, we advocate the usage of advanced probe card technology that allows to directly probe on these micro-bumps. This paper reports on the technical and economical feasibility of this approach.

**Small-Pad Probing on 40 µm Al/Cu Pads Over Temperature**
Presenter: Koby Duckworth, Cascade Microtech (Co-Author: Daniel Ouellette, IBM)

Leading-edge device characterization relies on the precise, repeatable measurement of very small values. The test system contribution to any measured values must either be insignificant when compared to the device measurements, or be highly predictable. In addition, time to market pressures drive engineers to test early device prototypes as soon as possible. However the challenge with early testing is the fact that most fabs currently use copper as their normal interconnect metal. Copper is difficult to contact reliably under the best of circumstances and when testing occurs at elevated temperatures concerns about oxidation as well as contact resistance have driven most OEMs to cap their copper interconnects and pads with aluminum. This process adds time, risk, and variation to devices to be tested. This paper will explore the alternatives available with today’s characterization systems for bare copper, multi-temperature testing on small pads using simplified macros for in-test de-embedding and processing monitoring.

**Improving Signal Integrity through Advanced Probe Card Design and Advanced Probe Card Metrology**
John Strom, Rudolph Technologies and Jeff Arasmith, Cascade Microtech

The market trends for smaller diameter pads, pillars and bumps, and also for higher bandwidth or better signal integrity present challenges to probe card design. Probes with small diameter probe tips provide new capabilities for testing small pad/bump geometries. Short probe tips bring the space transformer closer to the device under test (DUT), but provide challenges to probe card metrology tools. While shorter tips improve signal integrity, the reduced distance from the probe tip to the space transformer challenges the probe tip recognition system in metrology tools. Smaller diameter tips also make visual tip recognition more difficult and they are more sensitive to force and displacement during contact for electrical measurements. When using a monolithic probe core, all the probe tips are overdriven together. This can cause the core to be damaged if it is not fully supported and probe tips are overtraveled individually. Probe card metrology tools face unique challenges to fully characterize individual probe tip positions and electrical properties without damaging the probe card. This presentation will describe how to achieve optimum signal integrity when testing emerging device technologies using advanced probe cards and probe card metrology tools.

**TRACK 2: OVERCOMING CHALLENGES OF SUB-THz PROBING**

**On-Wafer Antenna Probes at Sub-THz Frequencies**
Presenter: Jerry Shiao, National Nano Device Laboratories (Co-Author: Guo-Wei Huang, National Chiao Tung University)

As sub-THz applications are emerging in both academic and commercial markets to date, MMICs [monolithic microwave integrated circuits] have become critical RF devices to develop associated products. However, MMIC pads for signal transmission cause great difficulties in on-wafer testing and packaging at such frequencies. Thus, on-chip antennas have been widely suggested to be a better solution at sub-THz signal transmission. To measure these on-chip antennas at the wafer level, we have designed antenna probes at 330-500 and 500-750 GHz to receiver or transmit signals. These probes can be used in both near- and far-field regions due to their compact sizes. While they precisely cover the antenna beam and minimize surrounding interference, the probes are mounted on general probe stations. We have tried several methods to develop new calibration. The on-chip antennas are slot antennas, which can pass modern semiconductor process design rules. This presentation will introduce our antenna probe design, measurement setup, calibration method, on-chip slot antennas, simulations and measurement results.
Development of Compact VNA Extenders to 750 GHz
Jeffrey Hesler, Virginia Diodes
Virginia Diodes has developed a series of VNA extenders with significantly reduced size that maintain state-of-the-art performance, and are thus well suited for on-wafer probing. For example, the volumes of the extenders from WR-15 (50-75 GHz) thru WR-5.1 (110-170 GHz) have been reduced by 75% while retaining the same dynamic range (120 dB typ.), stability and test port power. In addition, a WM-380 (WR-1.5, 500-750 GHz) extender with reduced size has been developed, enabling 4-port on-wafer measurements up to 750 GHz. Performance and measurements using these extenders will be presented at the conference.

Techniques to Evaluate RF Test Cell Repeatability and Accuracy
Gavin Fisher, Cascade Microtech
Modern device models rely heavily on extractions based on S-parameter measurements. As a part of the Wafer-Level Measurement Solutions offering from Cascade Microtech and Keysight Technologies, it was necessary to conduct a rigorous study of RF test cell accuracy and repeatability at 26.5, 50, 67 and 110 GHz at ambient and at elevated temperature. In this presentation, we will discuss the methods that can be employed using the WinCal XE™ calibration software and comparatively simple coding using Microsoft .Net’s programming environment. Armed with these tools it was possible to evaluate:

* Variation of calibration coefficients from multiple calibrations at single or multiple calibration sites
* Variation of computed open response from single or multiple calibration sites
* Variation of measurement response of independent line standards not used during calibration and of significantly different impedance
* System drift with time
* Standard lifetime

These methods were essential to benchmark system performance, and in one test case, highlighted a system setup issue which otherwise was not immediately apparent from calibration verification alone.

TRACK 3: ADVANCED TECHNIQUES

Improvements in On-Wafer MMICs Testing through ATE System
Antonio Nanni, Selex ES
Selex ES has developed a substantial degree of competitiveness in the design and production of microwave and millimeter-wave systems. This competitiveness is based on high skill competence related to the fabrication, design and RF testing of power GaAs and GaN MMICs. In particular, the capability to test MMICs at the wafer level through Automatic Test Systems (ATE) is mandatory to reduce manufacturing costs, time and improve yield. The developed on-wafer ATE allows 100% on-wafer RF screening of millimeter-wave MMICs, HPA-DA-LNA. The physical implementation of the on-wafer test system is based principally on a semi-automated Alessi REL-6100 station, a non-linear vector analyzer and a Noise Figure Analyzer. The test software is based on LabView and allows to communicate directly with the chuck controller and all measurement instruments, through GPIB commands. The test software is modular, making it easily adaptable to requirements and it is attached to a linked database for rapid data analysis and chip delivery. Through these features it is possible to test automatically HPA, DA and LNA up to 26 GHz on the entire wafers. The developed ATE system allows to reduce about 90% of the testing time, to reduce the chance of human errors and to improve accuracy.

Throughput Advantages of the Multi-Site Method for Wafer-Level Reliability
Presenter: Chih-Yang Chang, Applied Materials (Co-Author: Timothy McMullen, Cascade Microtech)
This case study evaluates two methods for performing wafer-level reliability (WLR) testing. Test results revealed a clear throughput advantage from full wafer, multi-site testing using Cascade Microtech’s Symphony WLR system with a semi-automated probe station and time dependent dielectric breakdown (TDDB) Modules, when compared to a single-site autoprober system. The experiment performs bias temperature stress (BTS) tests with multiple electric field values on advanced intra level dielectric (ILD) structures. Test data is reviewed to confirm correlation between the two test systems. This case study also considers tradeoffs between the methods such as flexibility, ease of use, and equipment cost.

Advances in Low-Frequency Noise Measurements
Roberto Tinti, Keysight Technologies
Flicker noise and random telegraph noise (RTN), often collectively known as low-frequency noise, has long been considered critical characteristics of electronic devices. It significantly affects performance of a number of basic building blocks of analog, RF, and memory circuits. It is also a key indicator of process and material quality in semiconductor manufacturing. As the semiconductor industry continues to advance new technologies, the need for fast, accurate and repeatable characterization of low-frequency noise has never been greater. This presentation will touch on the importance and physical causes of low-frequency noise, briefly explain the measurement process, and discuss various key design considerations that have gone into Keysight’s newest wafer-level flicker noise and RTN measurement system, E4727A the Advanced Low-Frequency Noise Analyzer. Sample measurement results from wafers of major semiconductor companies will be illustrated.
Test Methodology Adaptation for Electromigration Testing of Advanced Back-End-Of-Line CMOS Technologies
Kristof Croes, imec and Eric Wilcox, Cascade Microtech
As electromigration is a key reliability concern for back-end-of-line interconnects, test methodologies are well established, where standards exist for many years already. Electromigration is a current-driven process and today’s test methodologies thus consist in applying a constant current through the test line at elevated temperatures, while the voltage-drop over the line is monitored over time to electrically monitor void formation. For N10-technology nodes and higher, copper lines are surrounded by thick (~3 nm) and conductive metallic barriers at their bottoms and sidewalls. Such barriers allow for so-called current shunting, where, when voids are big, the current flows through these barriers. A consequence is that voltage-drops over void remain limited, even when high currents are applied. For advanced CMOS technologies below the N10-node, the above mentioned metallic barriers will a) need dramatic scaling or b) be replaced by non-conductive barriers. With such extremely thin semi- or non-conductive barriers, sending a constant current through the test line will induce a high voltage over voids. Such high-voltage drops are not happening in real products as chip performance is voltage-limited. Given the above considerations, we believe revisions of today’s electromigration test methodologies are appropriate, where we want to put forward constant voltage testing as a candidate to replace constant current testing.

TRACK 4: HIGH-POWER ON-WAFER DEVICE CHARACTERIZATION

On-Wafer GaN Power Semiconductor Characterization
Gary Simpson, Maury Microwave
Gallium nitride (GaN) is a wide band-gap material that has been used for LEDs since the 1990s. In recent years, its usage has spread to the power electronics community as a viable alternative for medium-voltage power conversion applications where IGBTs and MOSFETs have traditionally excelled. While GaN has many advantages such as Ron reduction at high breakdown voltages, high electron mobility, high temperature capability and low cost, it also has several disadvantages. Electrical performance degradation over time, including a decrease in the threshold voltage and an increase in the gate leakage current, can be caused from electron trapping after driving in saturation or hole trapping after driving near breakdown. Self-heating often leads to current collapse and a reduction in output power. Characterizing GaN technology becomes challenging, with short pulses required to study self-heating, and independent quiescent and hot bias control needed to study trapping. Measurements on-wafer become even more challenging, with simultaneous high voltage, high current and short pulses being delivered through wafer probes to the device under test. This presentation will discuss the challenges faced with characterizing 600-650 V GaN transistors, offer solutions, and review measured data.

High Current, High Temperature Measurement Setup
Klaus Kelting, Infineon Technologies
A measurement setup covering the temperature range of 0°C up to 500°C is presented. The system is based on a converted Summit™ 12000 probe station. It utilizes nitrogen gas as a protective (anti-oxidation) gas and as a coolant agent. A ceramic chuck prevents unintentional soldering events as well as accidental oxidation. It also prevents Eddy currents working against current direction of a current pulse. The maximum currents for this setup have not yet been found.

High-Voltage Discrete Device On-Wafer Capacitance Characterization
Presenter: Mehrdad Baghaie Yazdi, Fairchild Semiconductor (Co-Author: James Victory, Fairchild Semiconductor)
Accurate characterization and modeling of high-voltage discrete devices such as super junction MOSFETs and IGBTs is critical for power conversion system level simulation. Conventional discrete device capacitances such as the input capacitance CISS, the output capacitance COSS, and the reverse capacitance CRSS for power MOSFETs [CIIES, COES, CRES in IGBTs] greatly influence discrete device dynamic circuit performance, in particular the critical dynamic losses EOFF and EON and the gate charge characteristics. In particular CISS [CIIES] presents numerous challenges in an on-wafer environment due to the combination of the extracted gate to source [emitter] and gate to drain [collector] capacitances. The work in this presentation advances the state of the art through development of highly accurate high-voltage on-wafer capacitance measurement set-ups and techniques. The measurement set-ups are implemented for Cascade Microtech’s Tesla probe station in combination with the Agilent B1505A analyzer. Results will be presented for power MOSFETs and IGBTs ranging from 600 V to 1200 V.

Simplifying Instrumentation & Prober Configuration for On-Wafer Power Device Characterization
Lee Stauffer, Keithley Instruments
On-wafer characterization of high-power semiconductor devices involves several different types of measurements: on-state (high current I-V), off-state (high voltage I-V), and capacitance-voltage (C-V) at high bias voltages. Unfortunately, each of these measurements involves complex reconfiguration including different instrumentation, cabling, electrical connections, and probes. Operator safety cannot be compromised, and the goal of course is valid measurement data. Keithley will discuss ways to simplify the test setup between high-voltage I-V, high-current I-V, and high-voltage C-V power device measurements. Doing so will save time, increase measurement confidence, deliver optimal results, keep the operator safe, and reduce the risk of equipment damage. Specific attention will be paid to high-voltage C-V where optimal measurements can be especially challenging.
## Schedule

### Thursday, October 9, 2014

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<tr>
<td>18:30 – 20:00</td>
<td>Registration</td>
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<td>Welcome Reception</td>
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### Friday, October 10, 2014

<table>
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<tr>
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<tr>
<td>07:30 – 08:00</td>
<td>Registration and Breakfast</td>
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| 08:00 – 08:20 | Welcome  
Michael Burger, President and CEO, Cascade Microtech, Inc. |
| 08:20 – 09:20 | Keynote  
John Y. Chen, Vice President of Technology & Foundry Management, NVIDIA |
| 09:30 – 11:35 | Track 1: Fine-Pitch Probing  
(See page 2 for abstracts)  
Track 2: Overcoming Challenges of Sub-THz Probing  
(see page 2-3 for abstracts) |
| 11:40 – 13:10 | Roundtable Lunch                          |
| 13:15 – 13:55 | Featured Session  
Frank Fitzek, Professor and Chair of Communication Networks at the Technische Universität Dresden |
| 14:00 – 16:50 | Track 3: Advanced Techniques  
(see page 3 for abstracts)  
Track 4: High-Power On-Wafer Device Characterization  
(see page 4 for abstracts) |
| 17:00 – 18:30 | Networking Reception                    |

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