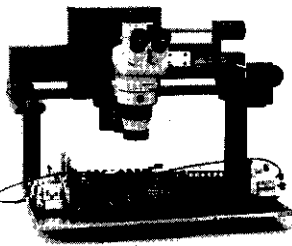


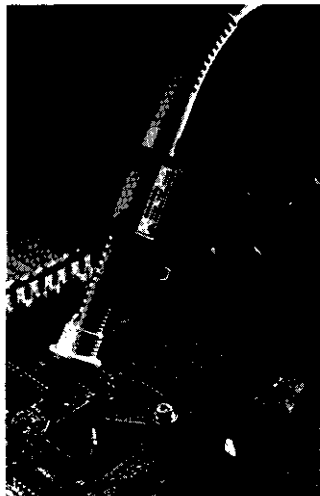
Microprobing Essentials for Fine Pitch Modules

A guide to probing today's high-speed, fine pitch technologies, including circuit boards, packages, high-density interconnects, and multichip modules.

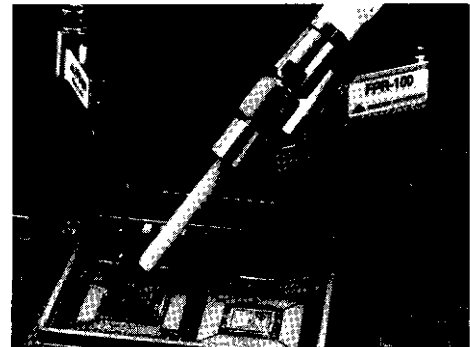
Hewlett-Packard Application Note 1242



Circuit boards and
high-density interconnects

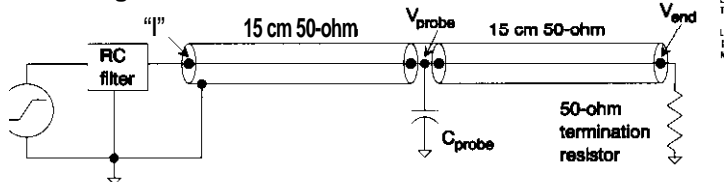


Surface mount technologies

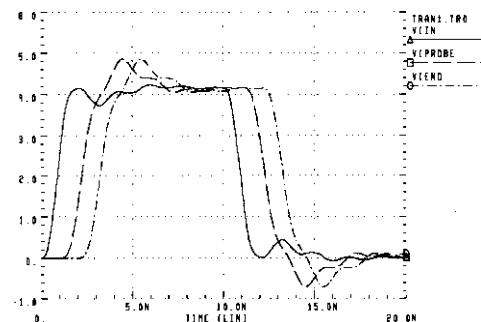


Multichip modules

Modeling



Simulation



Introduction

Today's new fine pitch surface mount technology (SMT) packages and multichip modules (MCMs) limit the usefulness of traditional handheld probes. At higher speeds, the problems can be electrical, but in general the limitations are mechanical. Just how do I electrically probe a fine pitch SMT device? With SMT pitches commonly 0.5 mm (20 mils) and 0.25-0.38 mm (10-15 mils) pitches soon, probing presents a serious problem for all users and manufacturers of SMT products.

Current solutions use the smallest available handheld probes, with one person performing the probing and another person operating the test equipment. Obviously, this inefficient approach has no future. Within the current spectrum of circuit probing capabilities (Figure 1), a large gap exists between handheld probes and wafer probers. Cascade Microtech is providing new techniques and equipment for this need. This application note describes the required essentials for making precise and accurate measurements on fine pitch circuit boards, packages, assemblies, and multichip modules.

Background

Three forces are creating an urgent need for fine pitch probing techniques:

1. Mechanical Circuit trace widths and pitches are continually becoming smaller.
2. Electrical Faster system speeds place unexpected demands on probing and grounding techniques necessary to achieve accurate electrical measurements.
3. Design philosophy Concurrent engineering and "design for test" techniques require complete subsystem characterization and qualification. Ever-increasing time-to-market pressure requires more rapid and accurate characterization feedback.

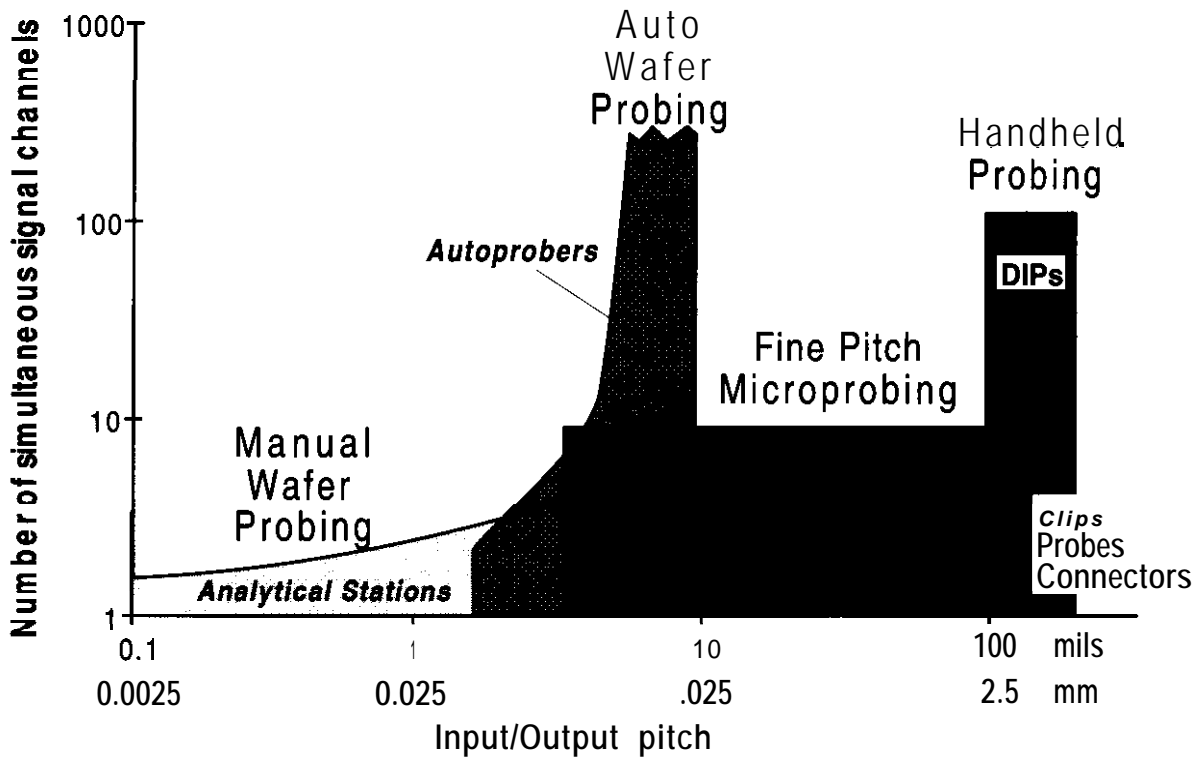


Figure 1. Spectrum of probing applications. New tools and techniques are filling the void between wafer probers and handheld probes.

Mechanical Considerations Figure 2 illustrates SMT and MCM input/output pitch trends. Just a few years ago, 1.25 mm (50 mils) and 2.5 mm (100 mils) pitches were the standard. Today, it is common to find 25, 20 and even 15 mil pitches. However, the practical limit of handheld probing is around 0.5 mm (20 mils). Placing a probe tip on a fine conductor located between two other fine conductors is difficult (Figure 3). Which conductor are you really on, and are you sure you haven't shorted two conductors together with the probe tip? This ambiguity is particularly intolerable when a large number of accurate measurements are required. No one will have confidence in the measured data.

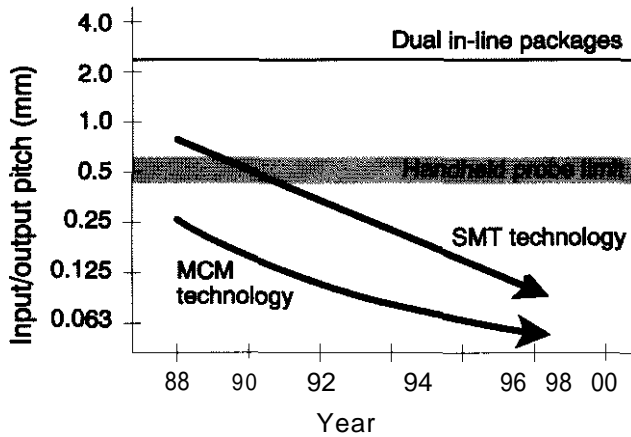


Figure 2. Input/output pitch trends for SMT packages and MCM modules.

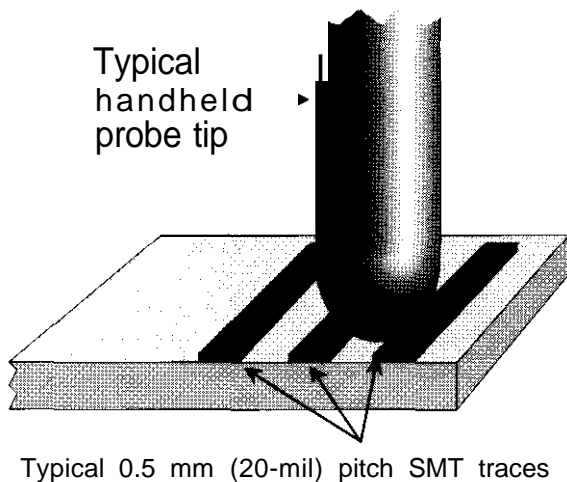


Figure 3. The handheld probing dilemma facing probes on fine pitch traces. Which line are you contacting?

Electrical Considerations The electrical performance of a handheld probe is generally considered perfect. After all, it's just a wire, what can go wrong? Try a simple example by hooking up a standard probe and scope to a fast step generator, and moving the ground lead (do not change the electrical connection). Note the difference in the displayed waveforms as you move the ground lead around. Which is correct and which will you believe? A probe is not really a perfect wire as many assume. Its bandwidth is finite and often very limited. For example, Figure 4 shows the step response of a typical handheld probe to a 35-ps step. This probe has a step response of 3.5 ns (100 MHz bandwidth), therefore it will only pass a 3.5-ns edge on to the measuring instrument, regardless of how fast the desired step is.

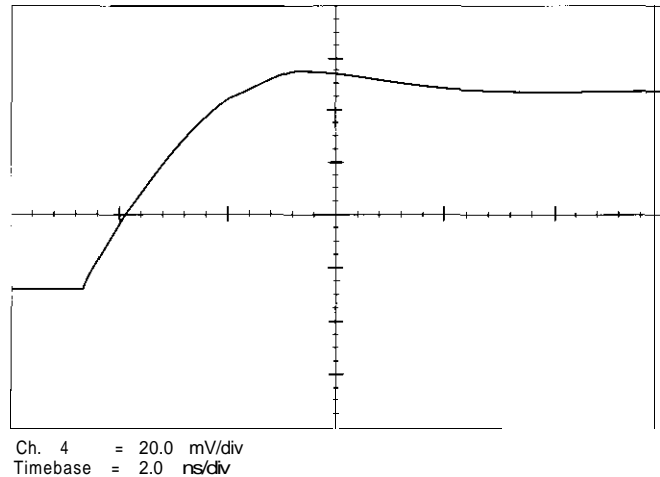


Figure 4. Standard handheld probe step response to a 35 ps step.

Probes present both a resistive (dc) and capacitive (ac) loads to the circuit under test. As expected, larger probes generally have larger tip capacitances that will affect the circuit being measured and result in measurement errors. As system speeds increase, handheld probes increase measurement errors that the test engineer may not realize.

Design philosophy considerations Engineers are increasingly pressured to complete design cycles more and more quickly. Concurrent engineering techniques were developed to meet these requirements, resulting in a greater emphasis on design for test and an expectation of "doing it right the first time." Many companies now perform complete characterization of

Microprobing Essentials for Fine Pitch Modules

their circuit assemblies, measuring noise margin and other critical parameters at every node on a large production sample. These companies often require verified “six sigma” performance, meaning all critical parameters will be 6 sigmas from failure. A great deal of testing is essential and the data must be accurate.

Accuracy Considerations

Several factors cause measurement errors, including probe limitations, cable losses, and cable reflections. In particular, there are four important sources of errors [1]:

1. The probe loads the circuit under test, altering the waveforms to be measured.
2. The probe's bandwidth is too small, distorting the signals passing through it.
3. Skin effect losses of even the best cables degrade transition times, adversely affecting settling time measurements.
4. A mismatch between the cable impedance and the instrument input impedance results in reflections, decreasing displayed waveform accuracy.

Probe loading effects Figure 5 illustrates the probe loading situation. In this case, a simplified output driver (modeled as a finite rise time source and output resistance R_o) drives several inputs (modeled as parallel R_s and C_s). An LRC circuit models the probe, with the variable inductance representing the variable-length ground. Ideally, the probe's effect on the circuit under test should be negligible, meaning that the voltage at the measured node will not change when the probe contacts it. However, this seldom happens when measuring subnanosecond transition signals.

Two aspects comprise probe loading problems—the dc resistive loading and the ac capacitive loading. Obtaining specific output driver IV curves and plotting load lines is the best way to analyze the dc loading [1]. In general, most bipolar and CMOS circuits tolerate 1 K-ohm loads (from a 20x probe) with little impact on dc levels. Many logic families specify output levels with a 500- or 1 K-ohm output load. Low-power logic families, however, often require the higher input resistance of the 100x probe (5K-ohms) or even 100K-ohm active probes (FPA-200).

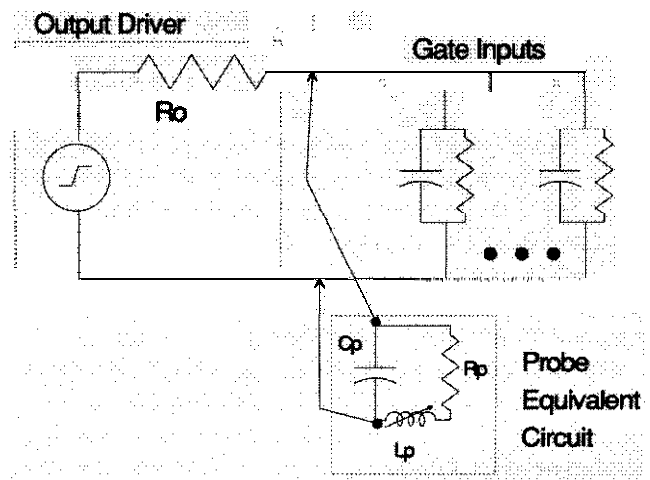


Figure 5. Typical digital circuit, with output driver, inputs, and probe equivalent circuit to evaluate probe loading effects.

The ac capacitive loading is more complex, because its impact on the circuit critically depends on the desired measurement. For example, if a simple transition time measurement is desired, most logic families will tolerate an extra pF loading with minimal change. However, when diagnosing a timing skew related glitch or metastable condition, then very slight timing changes on the critical clock nodes may prevent the phenomena from occurring. This is particularly frustrating if the glitch occurs only once every few hours.

A “quick and dirty” way of evaluating the effect of capacitive probe loading is to first connect one probe to the circuit under test, note the waveforms, then land another similar probe, and note the change in waveforms. If no change occurs, then assume that the placement of the first probe in the circuit had little effect on the circuit operation. This assumption is often valid for qualitative measurements, but not for solving critical timing problems.

A more analytical approach to ac probe loading examines how a capacitive load affects reflections in a transmission line. At system speeds of 50 MHz and above, circuit board and module interconnects are designed as transmission lines to maximize signal integrity. The capacitive loading of a probe results in significant reflections, distorting the original signal. The degree of distortion depends on the signal transition time and the capacitive loading due to the probe. A simple way of modeling this effect using HSPICE™ is shown in Figure 6. A probe contacts the midpoint, where two 15-cm lengths of 50-ohm transmission lines are connected. A variable transition time pulse is connected to the input, and the output is terminated in a 50-ohm resistor. The pulse source is connected to the transmission line by an RC filter (Figure 7) with lo-ohms series resistance, representing typical high-performance bus drivers. The RC filter eliminates the high-frequency components generated by the sudden transitions of an ideal ramp (Figure 7). These high-frequency components are not present in real waveforms, and thus result in simulation errors [2].

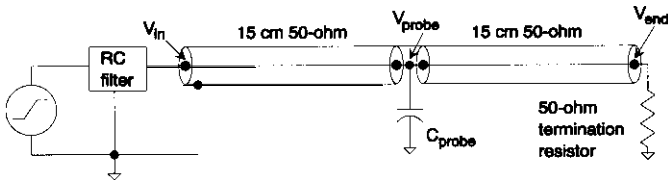
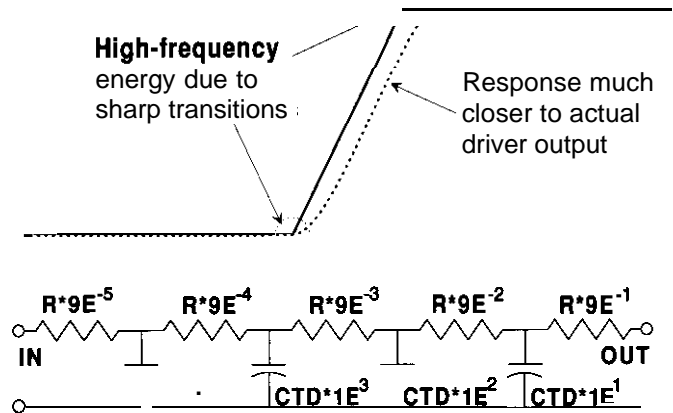


Figure 6. Transmission line model for analyzing effects of probe loading

This circuit was simulated using HSPICE with ideal transmission line elements, and using different values of probe capacitance and input signal rise time. With no probe capacitance and a 0.1 ns rise time, the response in Figure 6 was obtained, showing no signal reflections. However, with a 1 ns rise time signal, and 15 pF of probe capacitance, approximately 20% overshoot is present (Figure 9). Simulation results are tabulated in Table 1 for two values of overshoot: 2% representing high-accuracy characterization measurements, and 10% representing troubleshooting measurements.



$$CTD = TDFLT / (0.9 * RFLT)$$

where:

TDFLT = Filter time

RFLT = Output resistance

Figure 7. Source details of the transmission line model in Figure 6

Maximum reflection	Hand-held (15 pF)	FPA-Series (0.6 pF)	FPR-Series (0.25 pF)	FPM-20x (0.02 pF)
10%	> 2 ns	> 0.14 ns*	> 0.06 ns'	> 0.03 ns'
2%	≥ 10 ns	≥ 0.4 ns	≥ 0.2 ns	≥ 0.03 ns*

* Specification limit

Table 1. Recommended minimum signal transition times for traditional handheld probes vs. Cascade Microtech FP Series probes. These recommendations are based on the probe capacitance disturbing a terminated 50-ohm transmission line and causing either 2 or 10% reflection. For example, an FPR probe measuring a 0.2 ns edge in a 50-ohm environment will cause a 2% maximum reflection. When measuring slower edges, less reflection is caused.

Note that this simple analysis does not address all aspects of ac loading. However, it does provide the user with reasonably conservative guidelines for measuring high-speed signals in transmission lines.

Microprobing Essentials for Fine Pitch Modules

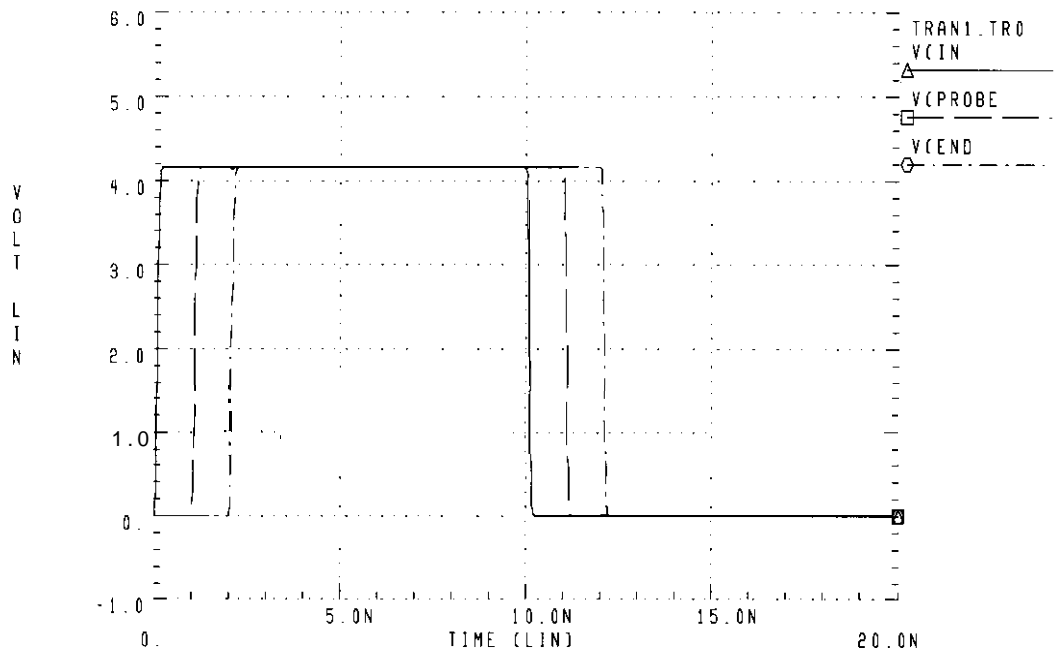


Figure 9. HSPICE simulation for schematic shown in Figure 6 (0.1 ns rise time, 0.02 pF tip capacitance)

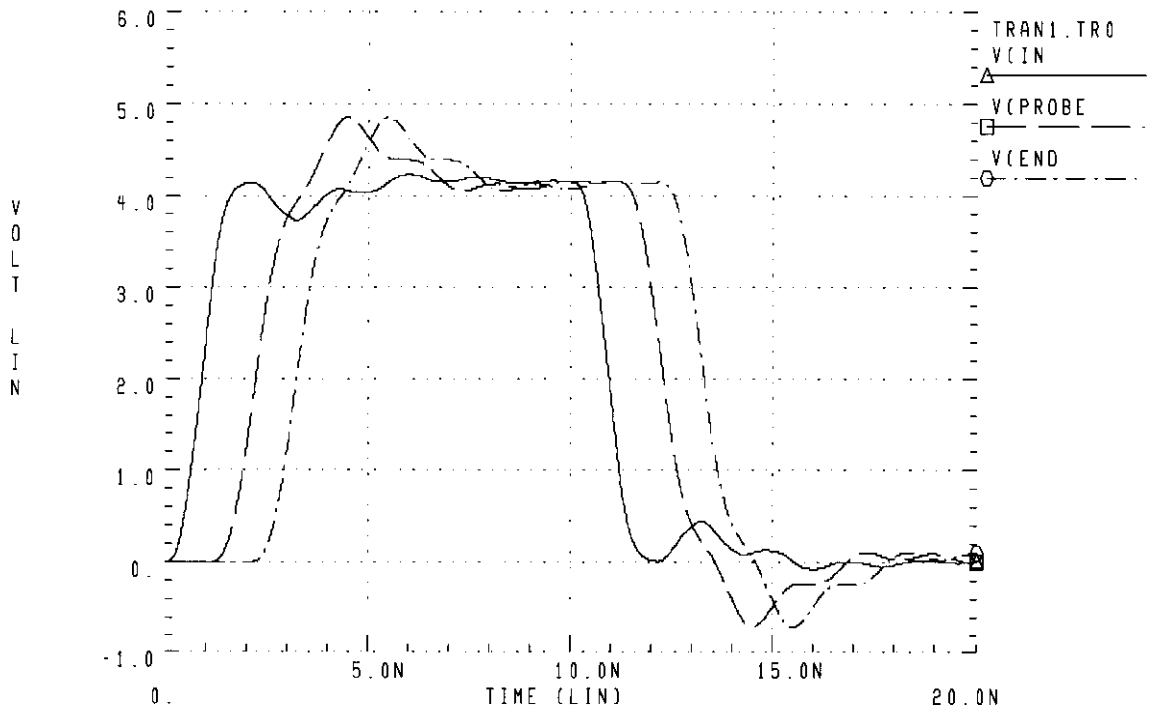


Figure 9. HSPICE simulation for schematic shown in Figure 6 (1.0 ns rise time, 15.0 pF tip capacitance)

Probe Bandwidth Limitations How much bandwidth do you need? As a general guideline, a square wave clock requires harmonics to 10 times its fundamental clock frequency to provide a well-defined edge. The total test system bandwidth should be at least as good and preferably 2-3 times better. Since a 100-MHz clock has significant harmonics to 1 GHz (Figure 9), your instrumentation must have a minimum of 1 GHz bandwidth and preferably 2-3 GHz. At first glance, this seems like overkill. However, the reason to measure is to find the unexpected and without sufficient bandwidth, the problem will go undetected.

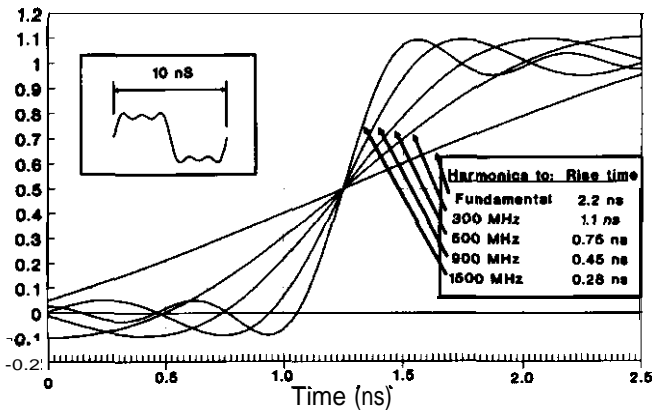


Figure 10. Frequency components of a square wave.

In the time domain, rise time is the critical parameter. When measuring rise time, Hewlett-Packard recommends that for 5% error, the combined rise time performance of the probe and oscilloscope must be $1/3$ the rise time of the signal being measured [1]. For 1% measurement error, the combined rise time performance must be $1/7$ the rise time of the signal being measured. The system rise time relates to the rise time of the system components by:

$$T_{rs} = \sqrt{(T_{r1}^2 + T_{r2}^2 + \dots)}$$

where T_{rs} = system rise time, T_{rx} = component rise time.

For example, to measure 1-ns transition times to 5% accuracy, then the combined probe and oscilloscope rise time must be less than $1 \text{ ns}/3$, or 333 ps. Assuming the rise time specification for the oscilloscope is 320 ps, then the probe rise time must be better than 92 ps or $(333^2 - 320^2)^{1/2}$. Both the FPM-Series (20 ps) and the FPR-Series (60 ps) probes satisfy this requirement.

A useful relationship for converting a specified system or probe bandwidth to rise time is [3]:

$$BW = \frac{.35}{T_r}$$

where BW = bandwidth in Hz, and T_r = rise time in seconds

The series resonant frequency of the probe's equivalent LC circuit limits the probe bandwidth, as a first-order approximation [1]:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

where C = probe input capacitance, and L = probe ground wire inductance. Violating this series resonance point will cause false overshoot and undershoot in measurements.

Figure 11 shows how increasing inductance or capacitance rapidly reduces bandwidth. A typical handheld probe with 15-pF input capacitance and a 7.5-cm ground lead is completely inadequate to measure current digital performance. Even high-performance handheld probes with 1-pF input capacitance and 5 cm ground lead offer only 1-GHz bandwidth (0.35 ns equivalent rise time). Measuring faster edges requires reduced probe capacitance and ground lead inductance. Because building low-capacitance probes is difficult, and since their ground leads are typically too long, this performance is beyond the capability of many handheld probes.

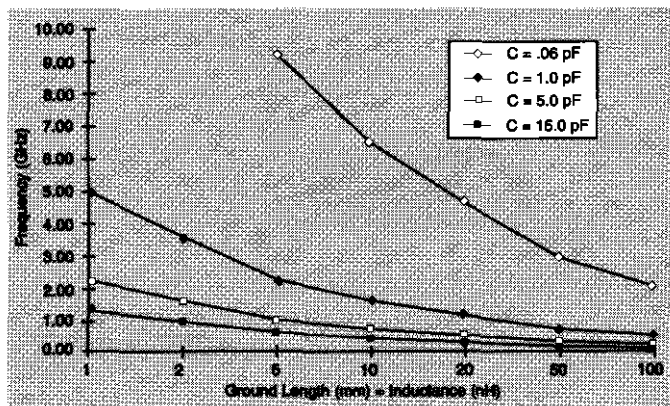


Figure 11. Probe resonant frequency vs. C and L.

High accuracy issues

High-accuracy (<2% error) settling time measurements require special care since the cabling can degrade the measurement more than the probe does. Two separate cable effects degrade settling time measurements: skin effect losses and cable/instrument reflections.

Skin effect With increasing frequencies, the current flowing in a conductor retreats to a “skin” at the surface of that conductor [4]. For copper, the skin depth at 1 GHz is 2.1 microns. With this effect, higher frequency components of digital signals attenuate more than the lower frequency components, thus degrading the step response. Figure 12 shows how skin effect degrades a 100-ps step through 2 meters of 20-GHz cable. Note that most of the initial step occurs rapidly, then near the top of the step, the response slowly settles to its final value.

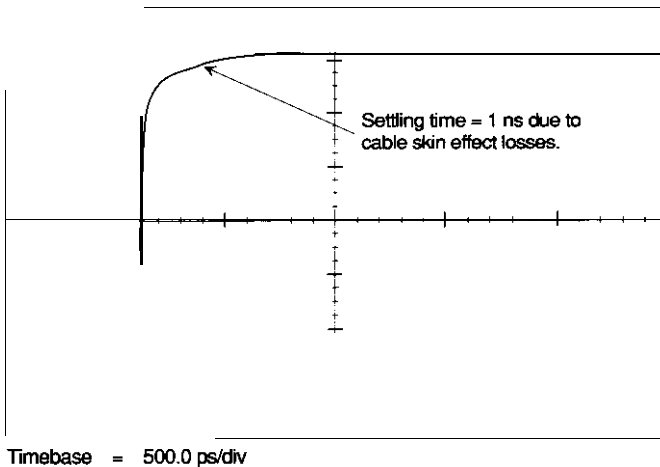


Figure 12. Skin effect step response degradation through 2 meter, 20-GHz cable.

Minimize skin effect in probe cables by:

1. Using as the shortest cable possible (<1 meter)
2. Measuring the cable step response to verify it is sufficient
3. Considering implementation of a correction/calibration algorithm to remove the effect of skin effect losses from the acquired data, such as the normalization function on the HP 54120 Series sampling oscilloscopes.

Cable/Instrument Reflections When the cable impedance and instrument impedances are not the same, reflections between the probe cable and instrument adversely affect settling time measurements. For example, if a 1 Ohm, 20x, or 100x probe is used to minimize circuit loading, the instrument input impedance is exactly 50 ohms, and the cable impedance is 51 ohms, then there will be a ripple effect (Figure 13) after each measured transition related to the impedance mismatch and the length of the cable. Given a 1-meter cable length, and a typical propagation delay of 5 ns/meter (for 50-ohm cable), then the amplitude of the first ripple will be around 1%. A 10-ns reflection will travel from the cable/instrument interface to the cable/probe interface and back to the instrument.

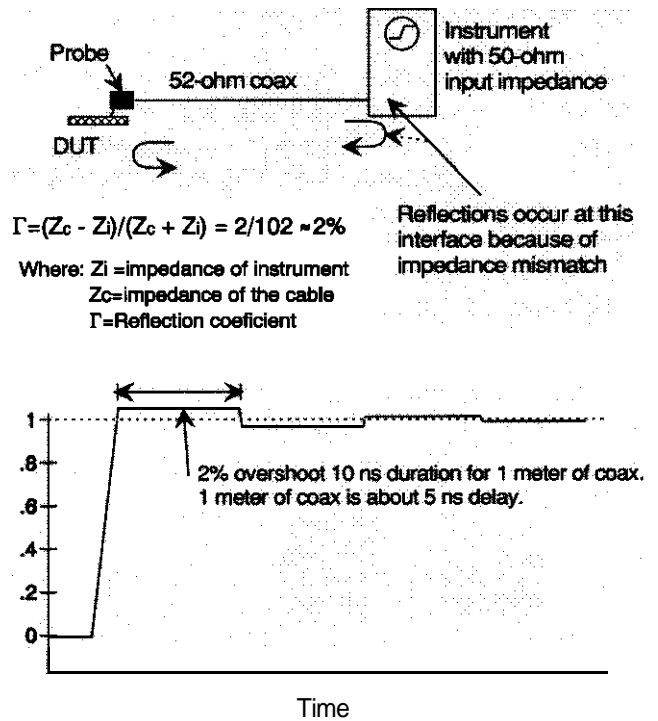


Figure 13. Reflections caused by cable/instrument impedance mismatch may impact settling time measurement accuracy.

To reduce instrument/cable reflections:

1. Select cables precisely impedance-matched to your instrument
2. Implement calibration/correction techniques to remove these effects from the measured data.

Layout Requirements

These test pad layout requirements should be used when probing with Cascade Microtech's FPM-Series Fine Pitch Microprobes, FPA-Series Fine Pitch Active Probes, or Fine Pitch Resistor-Divider Probes. They include minimum pad sizes, pad height, and maximum ground pad to signal pad spacing.

Rules marked with an asterisk (*) are intended for FPM-Series only. FPA- and FPR-Series probes are less restrictive. Please refer to the MCM Test Point *Design* Rules application note for additional layout for testability details or specific rules for the XMP-Series 10x Module Probes. Most of these rules can be violated to some extent. Please call our applications engineers to establish the optimal layout for your application.

Rule 100 Test Pad Size The minimum test pad size is 0.05 x 0.05 mm (2 x 2 mils) and the recommended minimum size is 0.10 x 0.10 mm (4 x 4 mils) (Figure 14). Although pads smaller than 0.05 mm square can be contacted, probing becomes difficult below 0.05 mm.

Rule 101 Test Pad Pitch The minimum center-to-center test pad spacing is 0.15 mm (6 mils) (Figure 14).

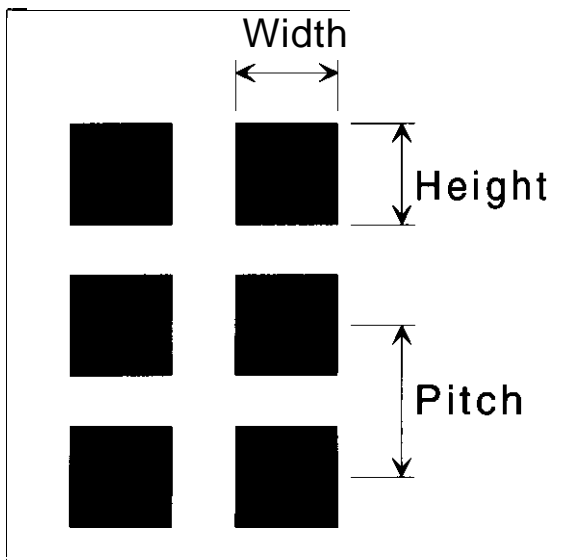


Figure 14. Minimum pad size and pitch design rules

Rule 102' Test pad height variation The maximum pad height variation between two pads being probed by the same probe unit (1 signal and 1 ground contact) is ± 1 mm (40 mils) (Figure 15). This value reflects the maximum vertical travel the FPM-Series' ground ribbon can make on the spindle and still make good electrical contact with it.

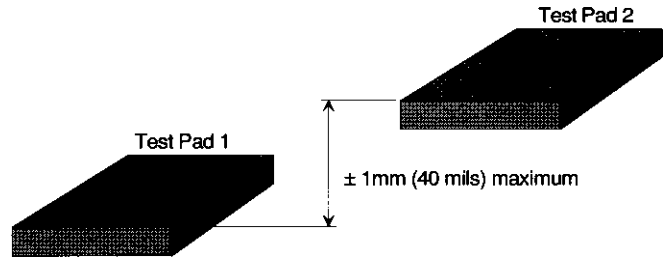


Figure 15. Test pad height variation design rule

Rule 103' Maximum Ground Pad to Signal Pad Spacing Ground pads must be located within 16 mm of every signal pad and node. This maximum value depends on the maximum FPM-Series probe ground ribbon length. Bandwidth of all probes degrades with increasing ground-signal pitch.

Rule 104* Ribbon clearance requirements Provide at least 1 mm FPM-Series ribbon clearance over components on the circuit board under test. Figure 16 details the clearance dimensions required. Call Cascade Microtech if you have questions regarding this requirement.

FPM-Series side view

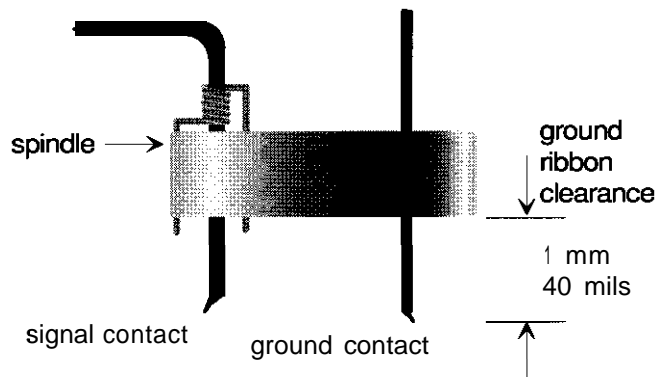


Figure 16. Ribbon clearance design rule

Microprobing Essentials for Fine Pitch Modules

Rule 105 Passivation Opening The passivation or conformal coating must be opened a minimum of 0.075 mm x 0.075 mm (3 x 3 mils) so the probes can make electrical contact with the pads (Figure 17). Coating thicknesses greater than 1 mil require larger openings to avoid the probe tip colliding with the coating. Call Cascade Microtech for specific details with respect to your project.

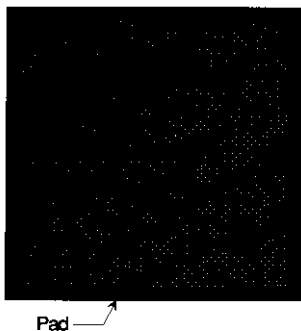


Figure 17. Passivation opening design rule

Recommended Layouts Cascade Microtech recommends the user develop a “layout designed for testability” philosophy. The general guidelines are to: 1) specify one test pad pitch and spacing, and 2) lay out all the signal pads oriented the same way in relation to the ground pads. Figure 18 shows a typical layout for MCM characterization with small, 0.15 mm (6 mils) pads, staggered to closely space the test pads. A

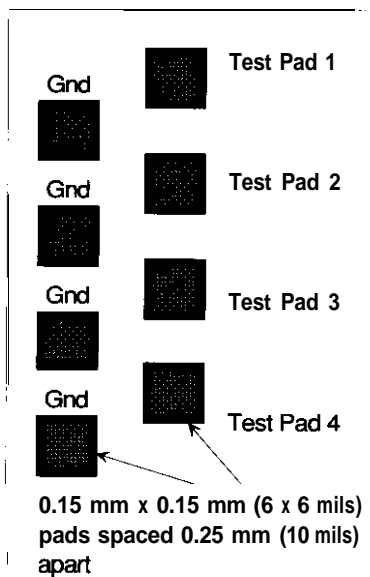


Figure 18. Typical MCM test pad layout

typical layout for SMT boards is shown in Figure 19 with 0.25 mm (10 mils) pads on 0.375 mm (15 mils) centers and a common ground bus. Note that in both of these examples each signal pad has a ground pad located the same distance and location from it. This means that when probing these test pads, test engineers do not need to reposition the signal contact with respect to the ground contact each time. The engineer instead moves the entire FPD-Series fine pitch positioner as a unit, quickly positioning the contacts on the next test pad set. Test pads should be grouped by signal type (i.e. all clock signals) and grounds should be marked so that power is not accidentally shorted to the ground probe.

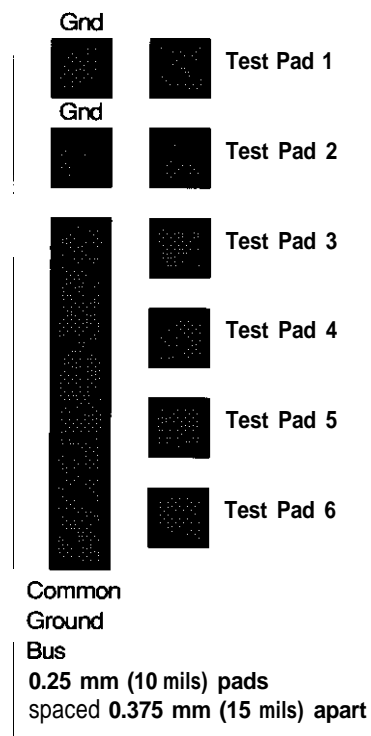


Figure 19. Typical SMT board test pad layout

Depending on specific testing requirements, it may be desirable to lay out test pads symmetrically about the center of the assembly, as shown in Figure 20. This is often useful when positioning probes over the entire board under test. If autoprobing is anticipated, consider orienting all test pads the same way. Probes can then be moved anywhere on the board without re-orienting signal and ground, as shown in Figure 21.

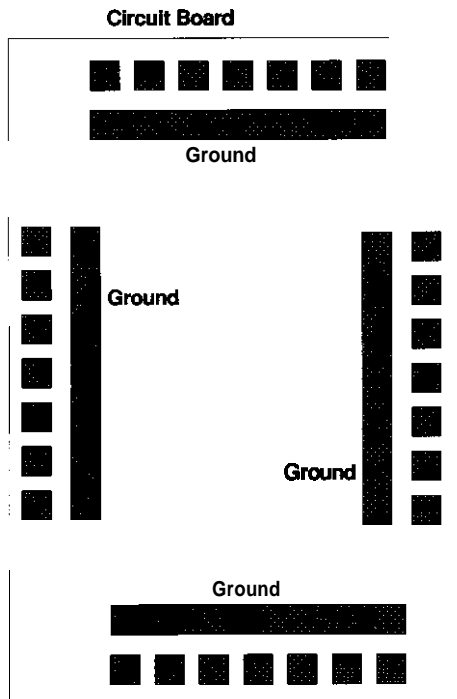


Figure 20. Test pad symmetry useful for manual probing using the MTS-2000 Fine Pitch Probing System

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- [2] *HSPICE User's Manual*, Meta-Software, Inc., Campbell, CA, 1991.
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- [5] *MCM Test Point Design Rules*, Cascade Microtech Application Note, 1992.

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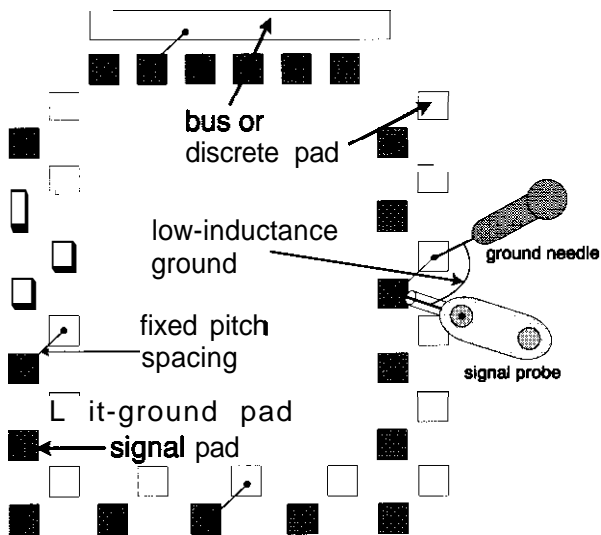


Figure 21. Test pad layout design using fixed pitch relationship between all pads for convenient autoprobing