Application Note

Low-Level DC Parametric Measurements for Process Device Characterization

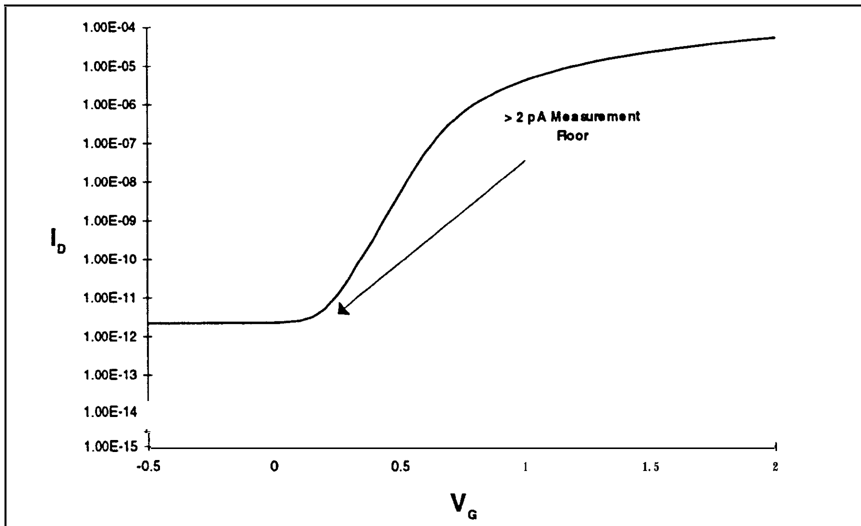

Figure 1. Measurement floor is limited at >2 pA due to measurement path probes, fixturing, and cabling.

Introduction

Ever-shrinking semiconductor device dimensions have necessitated reductions in power dissipation and signal levels, Characterization and reliability assessment of sub-micron devices have increased the need for precise and noise-free low-level measurements.

The measurement range and capability of semiconductor parametric test equipment has kept pace with process improvements in recent years. DC parametric analyzers now allow current measurements to femtoamp levels, while LCR meters provide femtofarad-level capacitance measurements.

However, many users find that the measurement accuracy of their complete on-wafer parametric test system is much more limited. While test equipment performance is very good, the fixturing of the device-under-test (DUT) and the wafer-probing system itself, often degrade the overall measurement performance. This application note examines the major causes of wafer-test system inaccuracy and recommends methods to improve overall system measurement accuracy and speed.

Examples of measurements and limitations

An examination of drain current in the sub-threshold region of the curve can quickly reveal drain, gate or and substrate defects. Detection of abnormal levels of sub-threshold drain current depends on the ability to make sub-pA measurements. It is not uncommon for the measurement floor to be limited to much higher levels. Since the drain voltage is set at several volts, there is the potential for DC leakage current in the drain-measurement line, reducing the measurement floor (see Figure 1).

Substrate **Current:** MOS substrate current is often monitored to assess gate hot-electron degradation as a means of screening for device lifetime. This substrate may be electrically connected to the metal of the wafer chuck on the probing system. The large chuck area acts as a large antenna which picks up electrostatic and electromagnetic noise (see Figure 2).

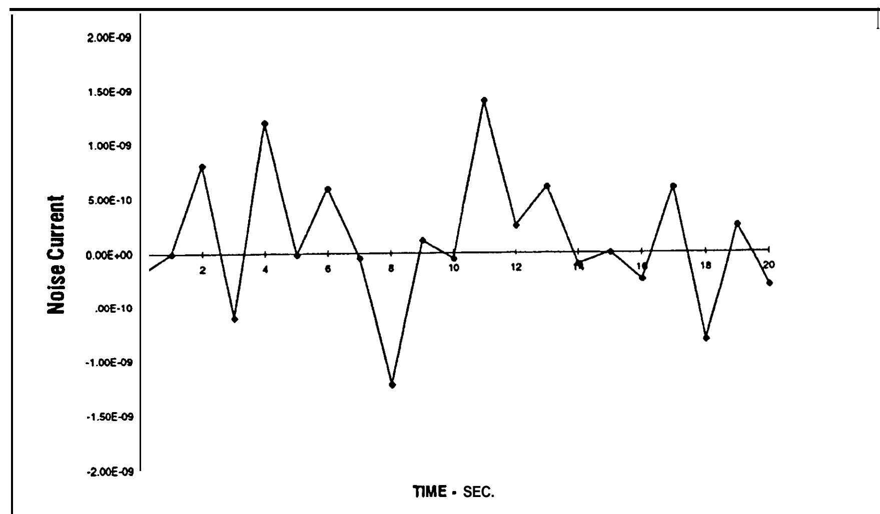

Figure 2. Random electrostatic and electromagnetic noise on a standard un-shielded chuck.

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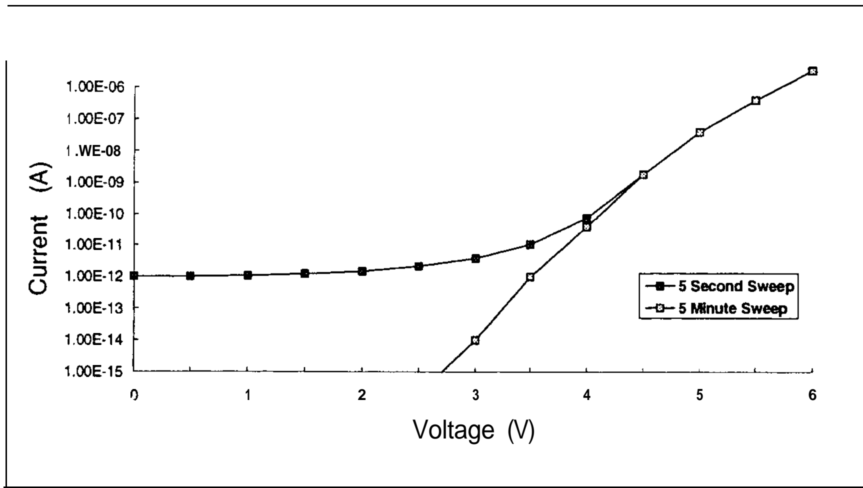

Figure 3. Very slow voltage sweeps are often needed to measure low currents.

Gate oxide leakage

Evaluation and characterization of increasingly thin insulating gate oxides is critical to the development and reliability of MOS VLSI technology. Low-field leakage is often measured following a high-field swept bias. Many users find that when measuring low-oxide leakage levels using a swept voltage, it is necessary to use a very slow sweep to achieve the necessary measurement floor. This result in very low measurement throughput (see Figure 3).

Limiting factors

System Current Leakage – High-resistance paths exist between the SMU (DC source monitor unit), the stimulus/measure path, and the ground. The paths may be in the material between a cable-center conductor and shield (ground), from the probe tip to probe holder, in connectors and couplers, and from the wafer chuck to the ground. This leakage current is parallel to the system's current measurement path and directly adds an error current to all current measurements. Current leakage in wafer-test systems often make it impossible to get accurate measurements below 1 nA. Figure 4 shows the parallel current-leakage paths in the triaxial cables, probes, and wafer chuck.

Stray Capacitance: Wafer probes, SMU cables, and the wafer chuck each represent a shunt capacitance to ground. This stray capacitance causes errors in both capacitance and DC current measurements. In capacitance measurements, the stray capacitance adds directly to the measured amount. The customary way of compensating for this residual capacitance is to null the C-meter with probes in the air. Nulling stray capacitance is only partially effective because it assumes constant capacitance. It is very typical for capacitance to vary widely depending on such factors as probe placement, vibration, temperature, cable strain, etc. (see Figure 5).

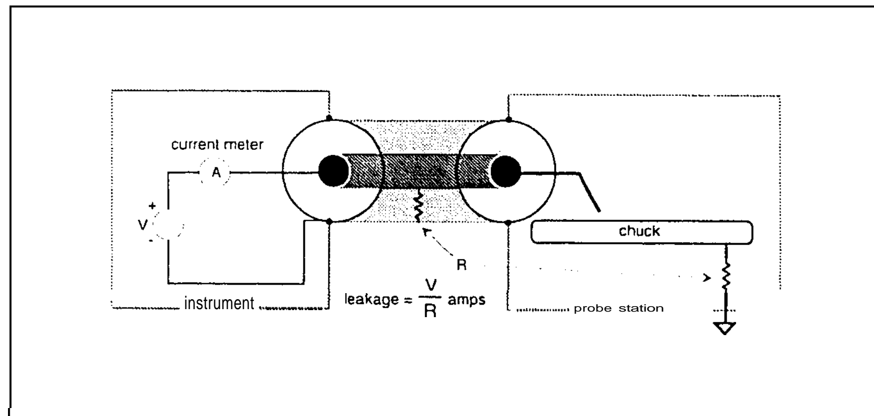

Figure 4. Parallel current leakage paths exist in cables, probes, and wafer chuck.

For DC current measurements, any residual capacitance becomes an element that must be charged each time a voltage is applied. If the charging or settling time is insufficient, the SMU will measure the capacitive-charging current along with the DC DUT current.

For low-frequency swept measurements, I,,,,, = C DV/DT. It is easy to imagine how, with 1 pF residual capacitance and a 1V/sec sweep, a 1 pA error would result. Therefore, Ierror is minimized by either reducing the capacitance or the voltage rate of change of the sweep. In attempting to eliminate these capacitive currents, some users will use slower sweeps with more measurement hold and delay, but this increases measurement time significantly.

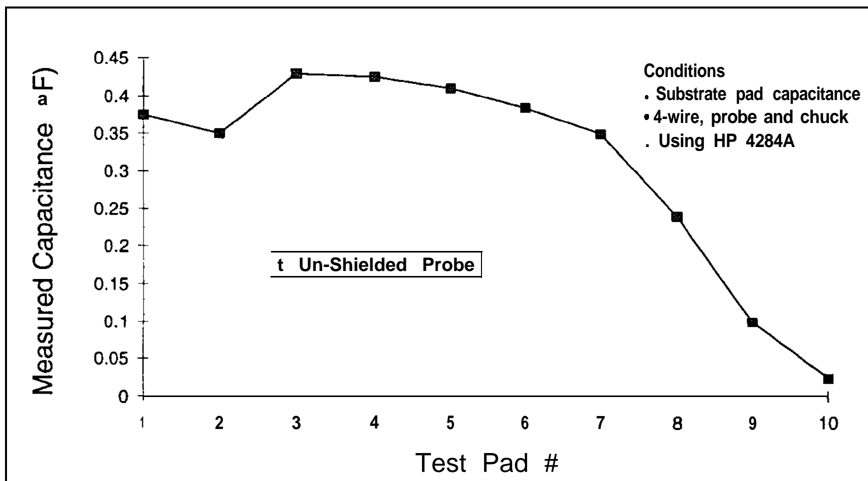

Figure 5. Capacitance may vary widely depending on probe location.

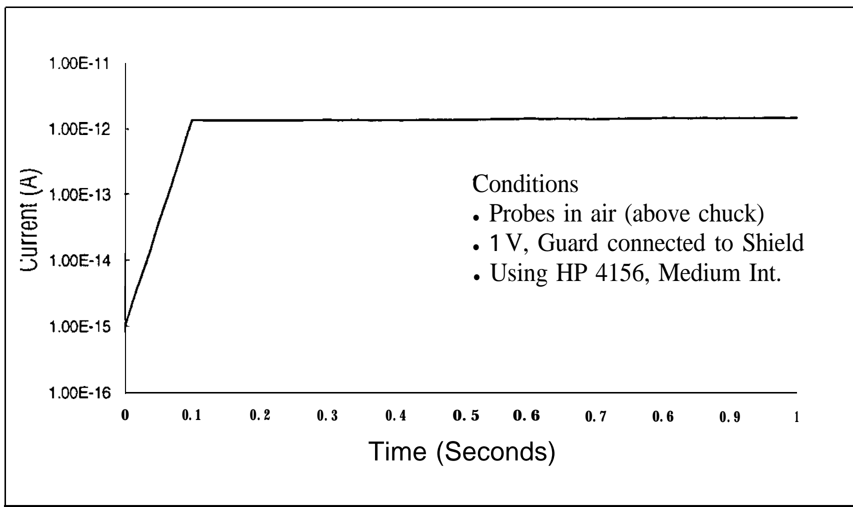

Figure 6. With probe in air capacitive current of over 1 **pA** still flows.

Figure 6 shows an open-circuit current measurement with a 4-second sweep, compared to an 18-second sweep. The faster sweep contains a DC capacitive-error current of about 700 fA, while the slower sweep provides adequate settling time so that measurements can be made down to the least significant bit of the measurement instrument (I fA).

Electromagnetic Interference: Magnetic fields passing through the signal path and the DUT are likely to generate error currents. When magnetic fields pass through the probes, cabling, and the DUT area, they generate stray currents which reduce measurement accuracy. These fields may be caused by motors, transformers, adjacent test equipment, or high-frequency sources like antennas. These low-level currents are measured along with the DUT current, and may overwhelm the measurement with noise at low measurement levels. In addition, the DUT itself may rectify an AC signal to produce a DC effect.

Electrostatic Interference: Static charges in the measurement vicinity can also limit low-level measurement capability. The current generated is proportional to the amount of coupling capacitance and the rate of change of the voltage. Therefore, as the charged object moves, or as the charge voltage changes, error currents are generated. This relationship is expressed as: electrostatic error current = CDV/Dt + V DC/Dt.

Series Resistance: Voltage measurement errors can occur even at moderate current levels if the DUT is in a low-resistance conductance state (<10W). This is due to IR drop in the conductance path. For example, signal lines and/or probes have as much as a l-ohm resistance. If the DUT is being operated in a low-resistance state with a low saturation voltage, then a significant voltage measurement error can occur. The error due to the IR drop becomes more significant when the ratio of stimulus-path-to-DUT resistance increases and whenever precise, low-voltage measurements are desired. Figure 7 illustrates the effect of series resistance in the force and measure path.

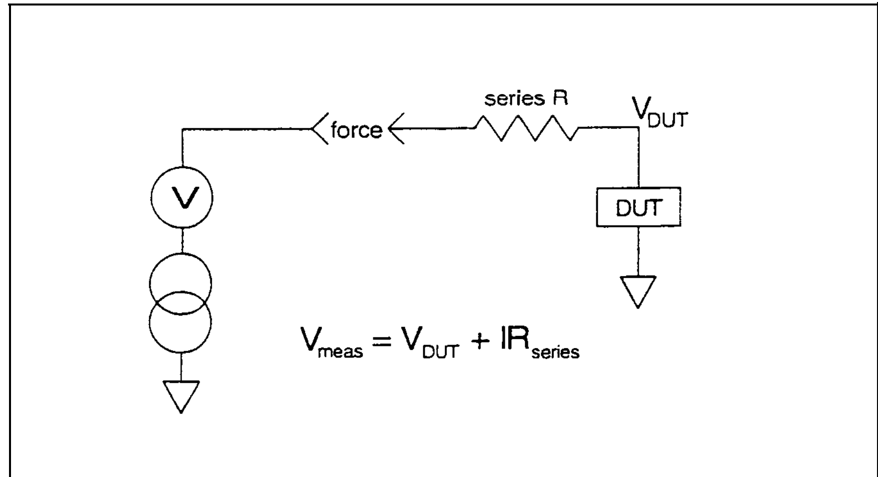

Figure 7. Voltage measurement error due to series resistance.

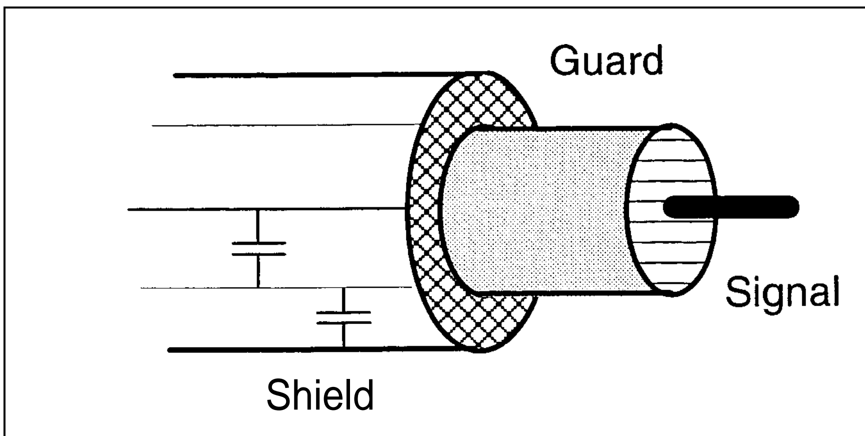

Figure 8. With triaxial cabling driven guard overcomes cable capacitance, and signal loss leakage.

Noise from thermal chucks

Reducing system-leakage currents: The first step in reducing system-leakage current is to take full advantage of the available test equipment architecture which provides triaxial outputs and triaxial cables. Figure 8 illustrates a cross-section of a triaxial cable. The triaxial cable has a special shield or guard between the inner conductor

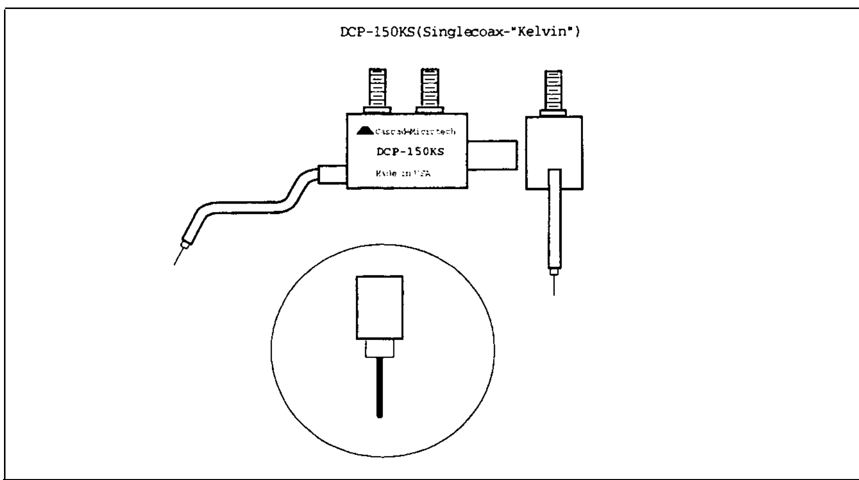

Figure 9. Coaxial probe with driven guard including needle arm is very low capacitance.

and the outer shield. The DC SMU connects a special driver to the guard. This guard driver maintains the guard at the same voltage as the center conductor. The low-voltage differential between the center conductor and guard is maintained whether the conductor is carrying a steady DC level or is swept. Keeping the guard and signal line at the same voltage effectively eliminates the ground leakage path in the cabling.

Improved wafer-probing system designs take advantage of this architecture by extending the driven guard into the measurement area. This includes providing probe guarding which connects to the SMU guard. Figure 9 shows a DC probe with the driven guard extending down the arm of the probe to a point near the tip.

For some measurements, such as substrate currents, wafer chuck bias may also be needed and current through the chuck may be measured. Traditional probe stations with isolated chucks often exhibit 1 nA or more of current leakage at 1 volt. Therefore, chuck guarding, as shown in Figure 10, becomes important to eliminate leakage paths through the chuck. By using a guarded chuck and connecting the chuck guard to the SMU guard terminal, chuck leakage paths are eliminated.

Stray capacitance: Properly-used instrument SMU guards not only reduce leakage, but can minimize capacitive error currents in DC measurements and reduce measurement time. As mentioned previously, when the DUT voltage is changed, stray capacitance must be charged. In a guarded system, the voltage in the triax cable guard follows any voltage change in the center conductor, greatly reducing cable capacitance and error current.

The same concept can be carried through to the probes and the chuck. By extending the SMU guard through to the probe tip, capacitance in the DUT area is reduced. The result is faster measurement settling times and/or sweep rates without capacitive error. Figure 11 shows an open circuit current measurement with a 5-second sweep both with and without the probe guard. With the probe guard, measurements can be made in the 20 fA to 60 fA range. However, without the guard, a 350 fA capacitive error current exists. At faster sweep rates, the error current would be even higher.

For capacitance measurements, guarding also plays a very important role. Stray capacitance in the cable, probes, and chuck area may

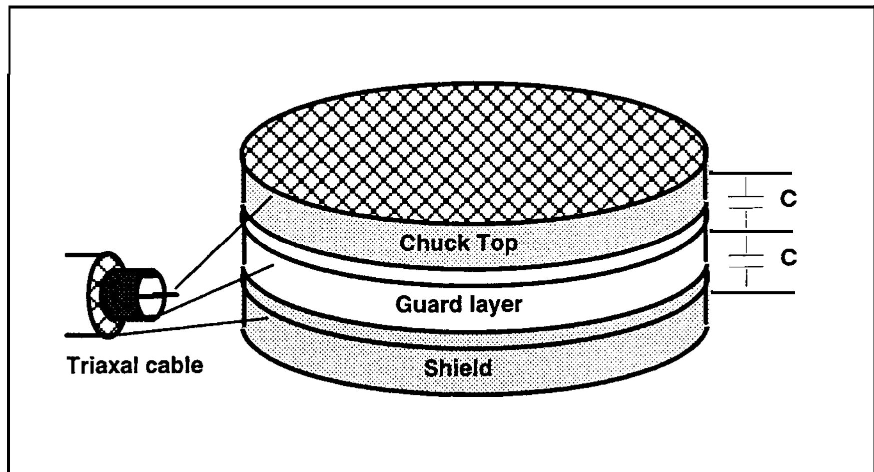

Figure 10. Driving guard layer to same potential as chuck (signal), stops leakage from chuck to the outside environment.

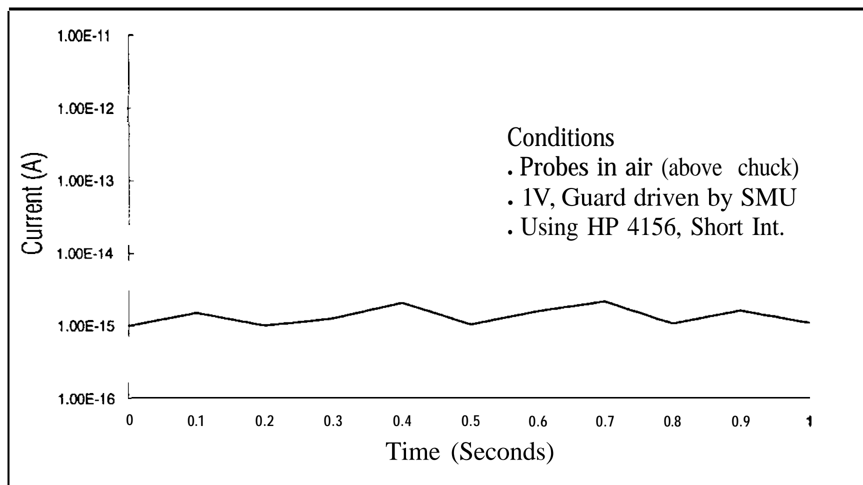

Figure 11. Capacitive error current is less than a few femtoamps with fully guarded probes.

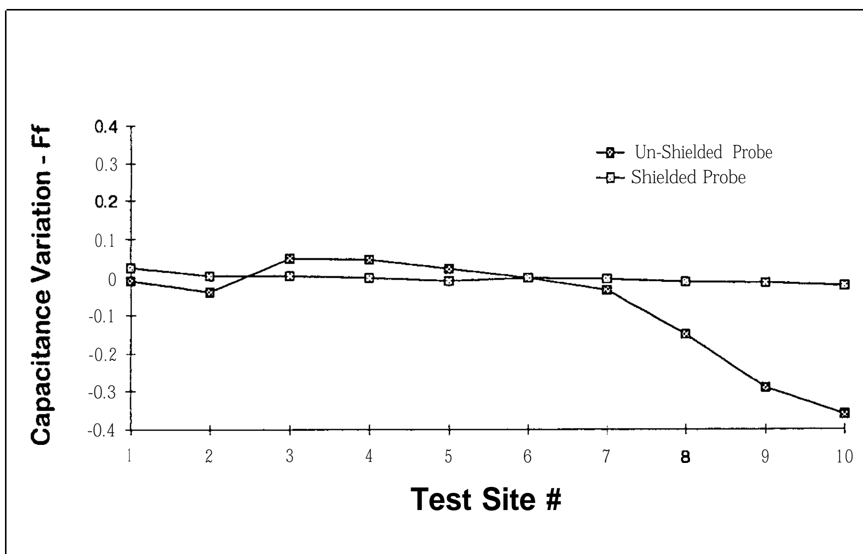

Figure 12. Fully guarded probe demonstrates very low capacitance variation with change in probe location over wafer and chuck surface.

overwhelm the desired measurement. Nulling out the capacitance is a partial solution. But, the problem with this approach is that if capacitive measurements are made in several locations over the wafer, the capacitance must be nulled for each site. Capacitance variation over the chuck surface becomes a limiting factor. By using guarded probes, chuck capacitance is not only greatly reduced, but is kept quite uniform over the chuck surface. Figure 12 shows how guarding reduces the capacitance variation with movement to various test sites on the wafer.

For capacitive measurements to the substrate, the chuck guard once again is very useful. The capacitance-meter HI-terminal's shield can be connected to the chuck guard with the LO terminals connected to the top of the wafer. This eliminates the capacitance from the chuck to the probe station's base.

Series resistance: The effects of cable and contact resistance can be virtually eliminated by using a system design that uses available SMU sense connections, as shown in Figure 13. This is accomplished by extending the high-impedance voltage sense connection to the wafer measurement point. Special two-point Kelvin sense probes are available for this purpose (see Figure 13).

Magnetic effects (electromagnetic and light): To reduce measurement susceptibility to electrostatic or magnetic fields, the entire measurement area must be shielded with a metallic partition or enclosure to control propagation to the measurement area. The smaller the enclosed volume, the better. Past solutions involved large metal enclosures which contained the entire probe station. This arrangement was not only cumbersome, but would not shield the measurement from the effects of an automated station's stage motors and other sources of 50/60 Hz radiation.

A more accurate and more convenient solution encloses only the wafer and chuck, leaving the noisy stage motors outside. Figure 14 shows Cascade Microtech's MicroChamber™-based parametric probe station. The MicroChamber provides the necessary shielding from magnetic effects. Other features of the probe station include full guarding and shielding into the device area to minimize leakage paths and convenient connections for low-level current and capacitance measurements.

On-wafer measurements over temperature

The typical -65 to +200°C thermal chucks create two problems which may compromise measurements; heater noise and high stray capacitance.

Heater Noise: Standard thermal wafer chucks use active devices for heating and cooling. When these devices cycle on and off, electrical noise is generated. Even at room temperatures, the heaters are active and noise is generated. Noise levels as high as 2 nA are not uncommon.

Capacitance: The multi-level solid insulating layers in the chuck are highly capacitive with typical values in the 1000 pf range. This results in long settling items following a

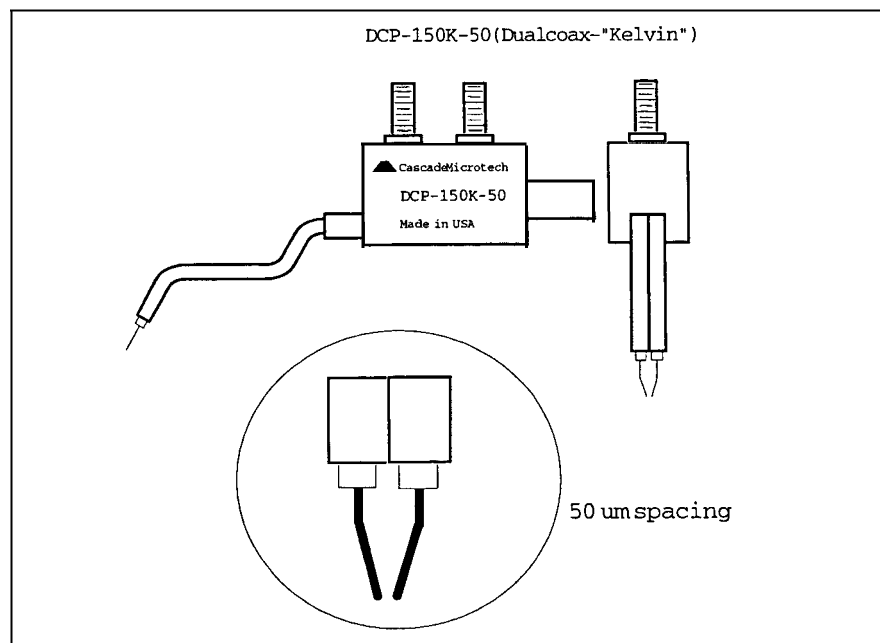

Figure 13. Dual-tip Kelvin probes eliminate the effects of series resistance in the signal path.

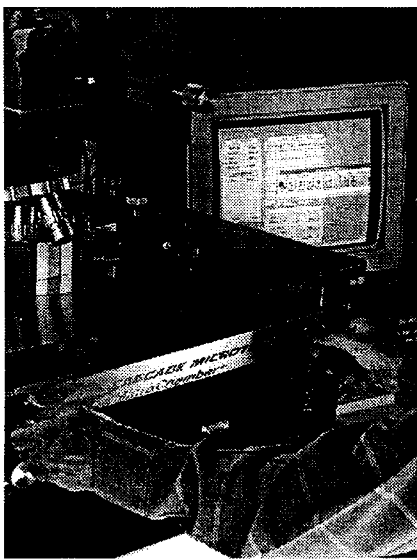

Figure 14. MicroChamber probes a dark, noise-free measurement environment and also serves as a Faraday shield.

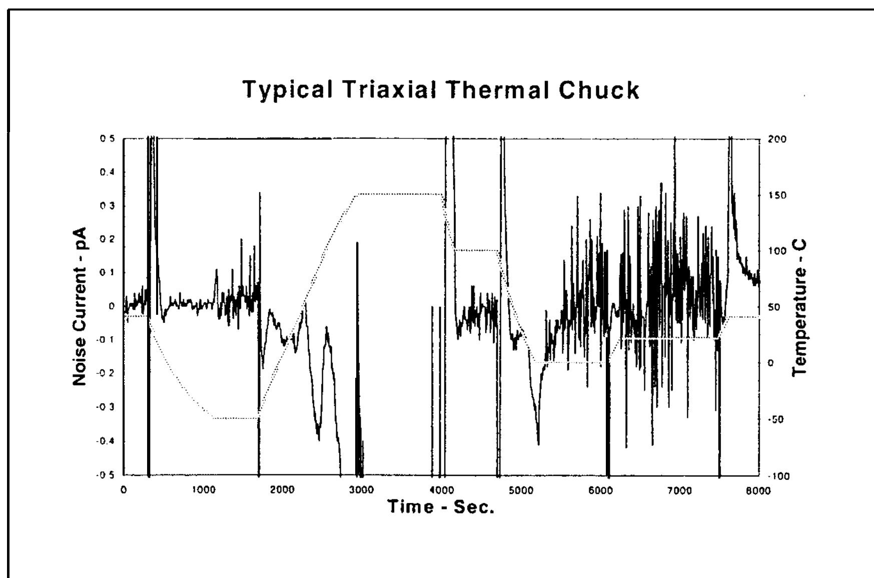

Figure 15. Typical low noise thermal chuck.

change in chuck/substrate bias.

Cascade Microtech offers thermal chuck probing systems which use two insulating layers with a guard layers sandwiched between. For current or voltage measurements, the guard is connected to the guard amplifier in the DC parameter analyzer. For capacitance measurements, the guard can be connected to the shield of the capacitance meter, eliminated parallel capacitance paths. The guard not only eliminates most of the interference from chuck heaters, but greatly reduces residual chuck capacitance. This produces a great improvement in heater noise on the chuck itself (see Figure 15).

Gain full access to your test instrument performance

The factors limiting wafer test system performance are well known. While parametric test instruments are addressing these factors, the remainder of the wafer probing system is often lacking. Through attention to electrical design detail, a wafer test system can be configured which allows you to use the full capability of your parametric test instruments. The benefit to the user is more accurate and faster parametric measurements.

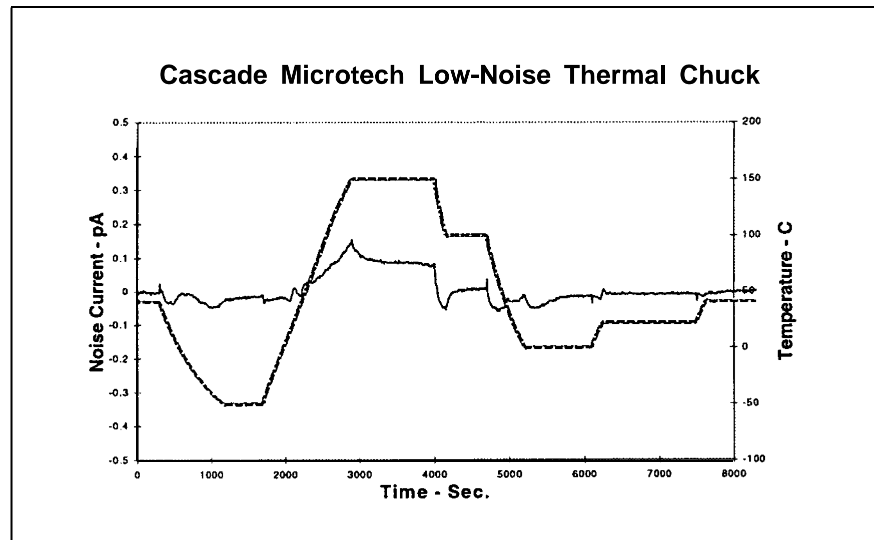

Figure 15. Cascade Microtech Alessi's MicroChambered Guarded low-noise thermal chuck.

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DCPAPP-0695