Measurement accuracy at mm-frequencies and beyond: on-wafer calibration vs. de-embedding techniques.
Who wins for THz SiGe HBTs?

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Outline

- Motivation
- Pad Parasitic De-Embedding Methods
- On-Wafer Calibration Methods
- Comparison Results
- Conclusion

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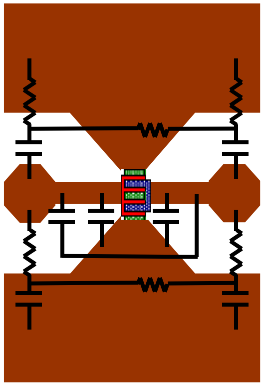
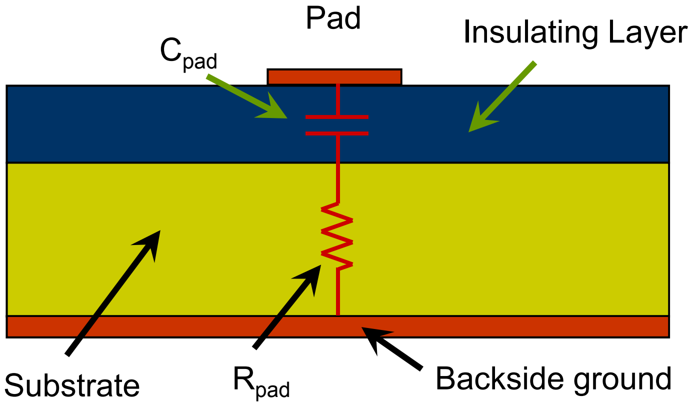
Transistor Measurement Challenges

- A transistor cannot be contacted (probed) directly:
  - Contact pads and interconnects are required
- Increase of measurement and operation frequency:
  - Impact of contact pads parasitics significantly increases





How to get rid of parasitics?

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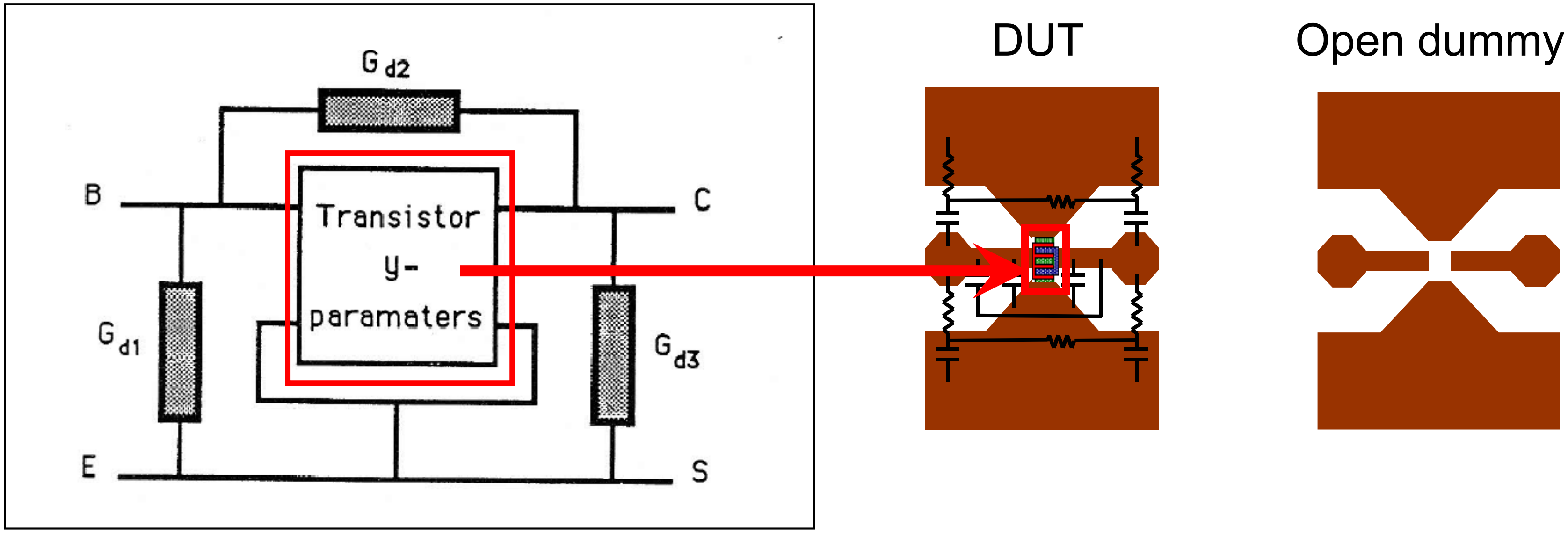
The First De-Embedding Method

- Introduced in 1987 for microwave HBT’s by van Wijnen
- Represent parasitics by an Open “dummy”
- Demonstrated results: up to 18GHz



The First De-Embedding Method

Measured Y-parameters Dummy:

$y_{11d} = G_{d1} + G_{d2}$; $y_{12d} = -G_{d2}$;

$y_{21d} = -G_{d2}$; $y_{22d} = G_{d2} + G_{d3}$.

Measured Y-parameters DUT:

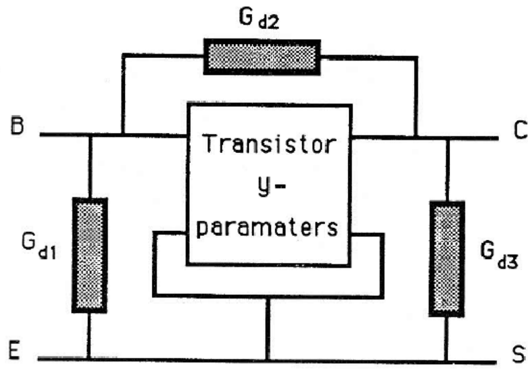
$y_{11m} = G_{d1} + G_{d2} + y_{11t}$; $y_{12m} = -(G_{d2} + y_{12t})$;

$y_{21m} = -(G_{d2} + y_{21t})$; $y_{22m} = G_{d2} + G_{d3} + y_{22t}$.

Corrected Y-parameters Transistor:

$y_{11t} = y_{11m} - y_{11d}$; $y_{12t} = y_{12m} - y_{12d}$;

$y_{21t} = y_{21m} - y_{21d}$; $y_{22t} = y_{22m} - y_{22d}$.



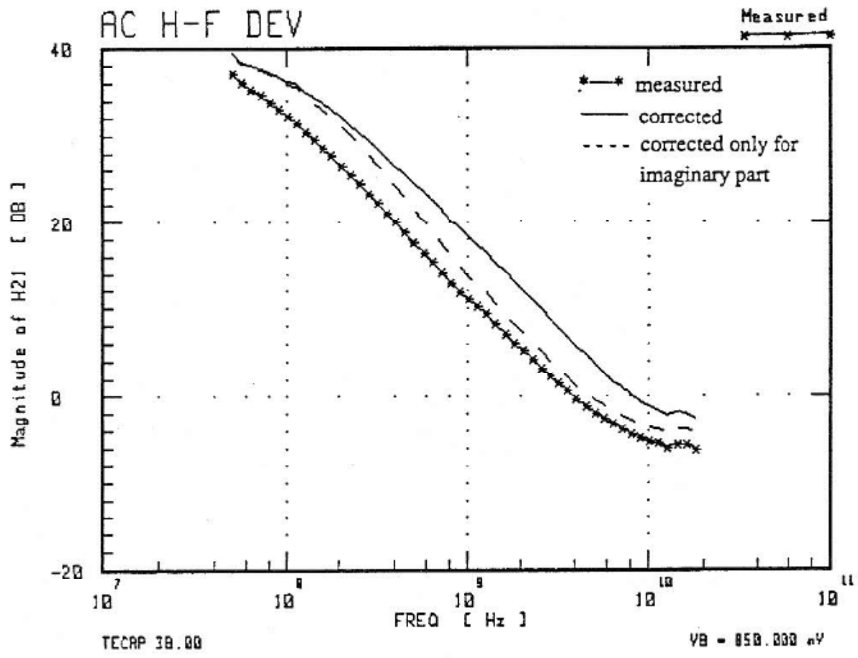


Figure 5. The magnitude of the ac-current gain, $|h_{21}|$,as function of frequency; (*) not corrected, (solid line) fully corrected and (dashed line) only the imaginary part corrected. (NPN Single base, $A_e = 7.2$ μm^2, $V_{ce} = 1.85$ V and $V_{be} = 0.85$).

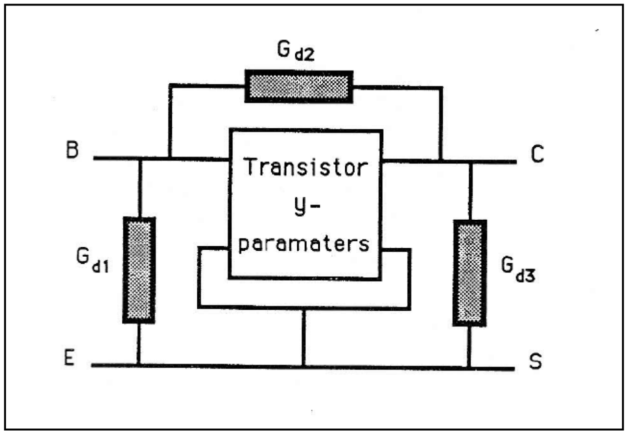
P. J. van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A new straight forward calibration and correction procedure for on-wafer high frequency S-parameter measurements (45 MHz–18 GHz)," in *Bipolar Circuits and Technology Meeting*, 1987, pp. 70-73.

Equivalent Circuit Methods

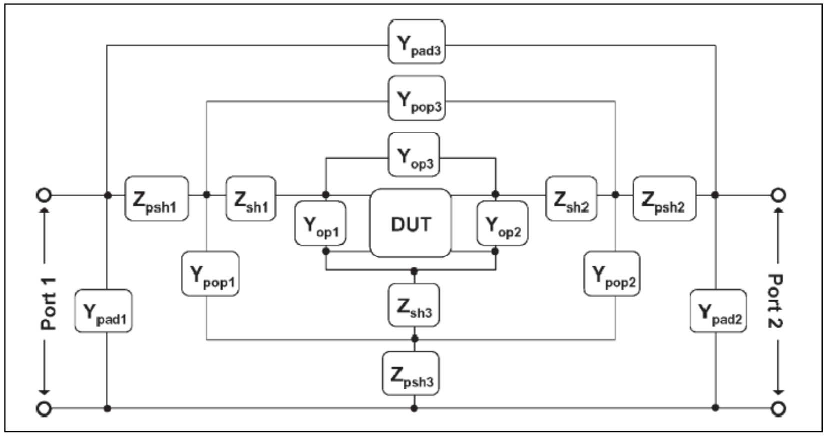
- With an increase of frequency, model complexity increases

One-Step (few GHz)

Five-Steps (<50GHz)



Frequency increase

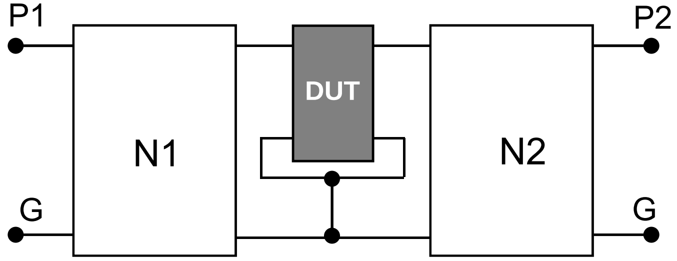


☹ Drawback: more dummies required

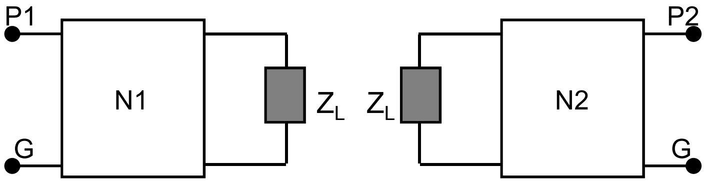
I. M. Kang, S.-J. Jung, T.-H. Choi, J.-H. Jung, C. Chung, H.-S. Kim, H. Oh, H. W. Lee, G. Jo, Y.-K. Kim, H.-G. Kim, and K.-M. Choi, "Five-step (Pad-Pad Short-Pad Open-Short-Open) de-embedding method and its verification," *Electron Device Letters, IEEE,* vol. 30, pp. 398-400, 2009.

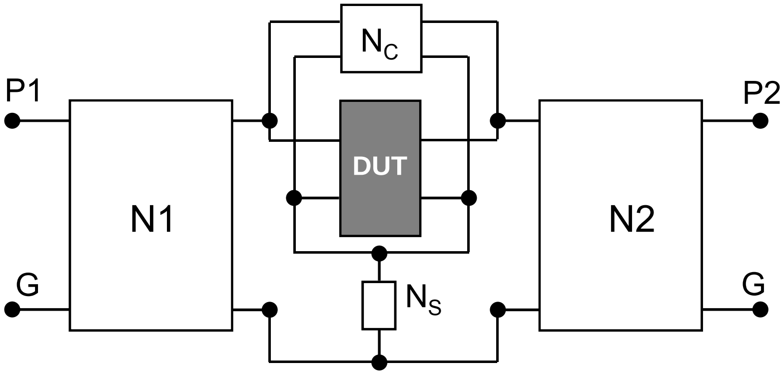
Cascade Matrix Methods

- Parasitics are represented as error networks N1 and N2
- Assumed reciprocity of N1 and N2
- N1 and N2 are defined from three standards:
  - Open, Short, Load
- Optional to define N_S and N_C:
  - SHORT and OPEN



$$T_{DUT} = T_1^{-1} T_{total} T_2^{-1}$$



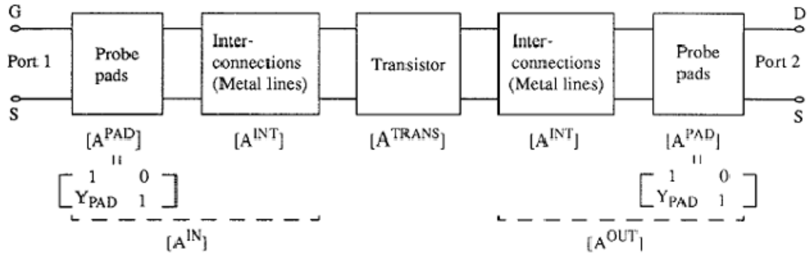


☹ Drawback: 5 dummies

J. Weng, "Error correction in high-frequency "on-wafer" measurements," in *Microelectronic Test Structures, Proceedings of the 1994 International Conference on*, 1994, pp. 164-167.

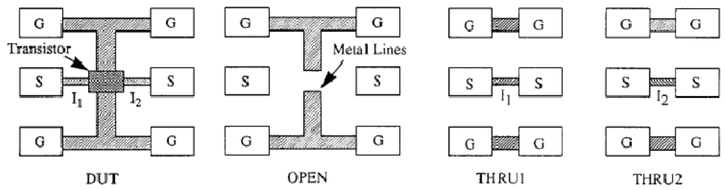
Cascade Matrix Methods: Open-½Thru1-½Thru2

- Only 3 Dummies:
  - Open, Thru1,Thru2
- Interconnect parasitics [A^{INT}] are measured by Thrus



☹ Drawback:

- Crosstalk when measuring ½Thru



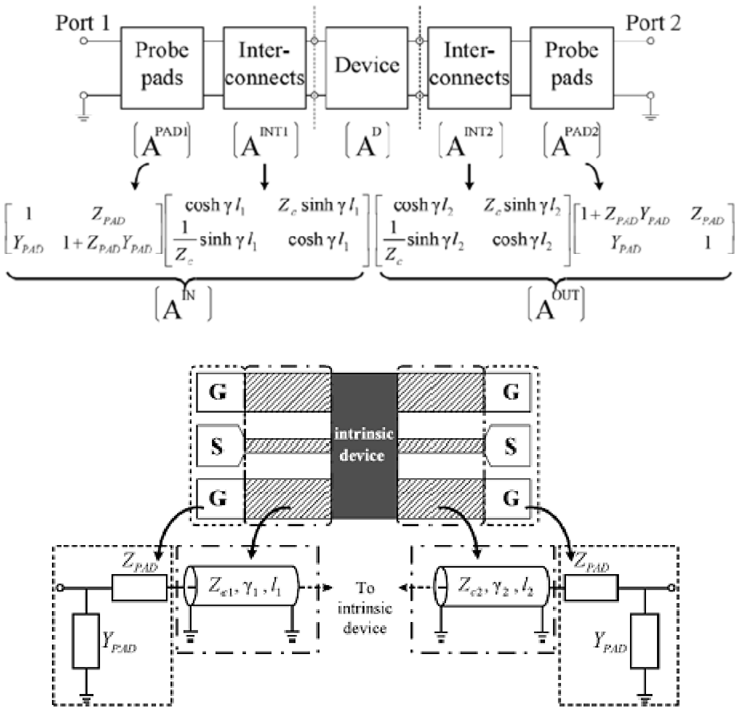
C. H. Chen and M. J. Deen, "A general noise and S-parameter deembedding procedure for on-wafer high-frequency noise measurements of MOSFETs," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 49, pp. 1004-1005, 2001.

Cascade Matrix Methods: Open-Thru; Open-Short-Thru

- Interconnect line characteristics Z_C and γ are extracted from Thru
- Pads influence Y_{PAD} and Z_{PAD} are defined from OPEN and SHORT

☹ Drawbacks:

  – Length of Thru

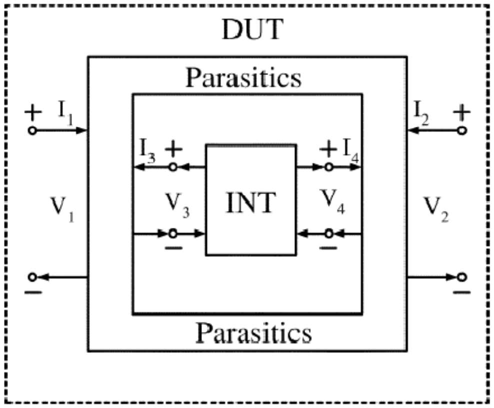


M.-H. Cho, G.-W. Huang, K.-M. Chen, and A.-S. Peng, "A novel cascade-based de-embedding method for on-wafer microwave characterization and automatic measurement," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, 2004, pp. 1237-1240 Vol.2.

M.-H. Cho, G.-W. Huang, C.-S. Chiu, K.-M. Chen, A.-S. Peng, and Y.-M. Teng, "A cascade Open-Short-Thru (COST) de-embedding method for microwave on-wafer characterization and automatic measurement," *IEICE Trans Electron,* vol. E88-C, pp. 845-850, May 1, 2005 2005.

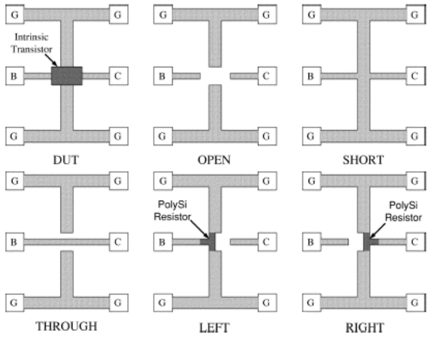
General Four-Port De-Embedding

- All parasitics are represented as an unknown 4-Port system
- I-V relationship for ports is given by 4x4 Y-matrix



☹ Drawbacks:

  - 7…3 standards
  - Standards must be known

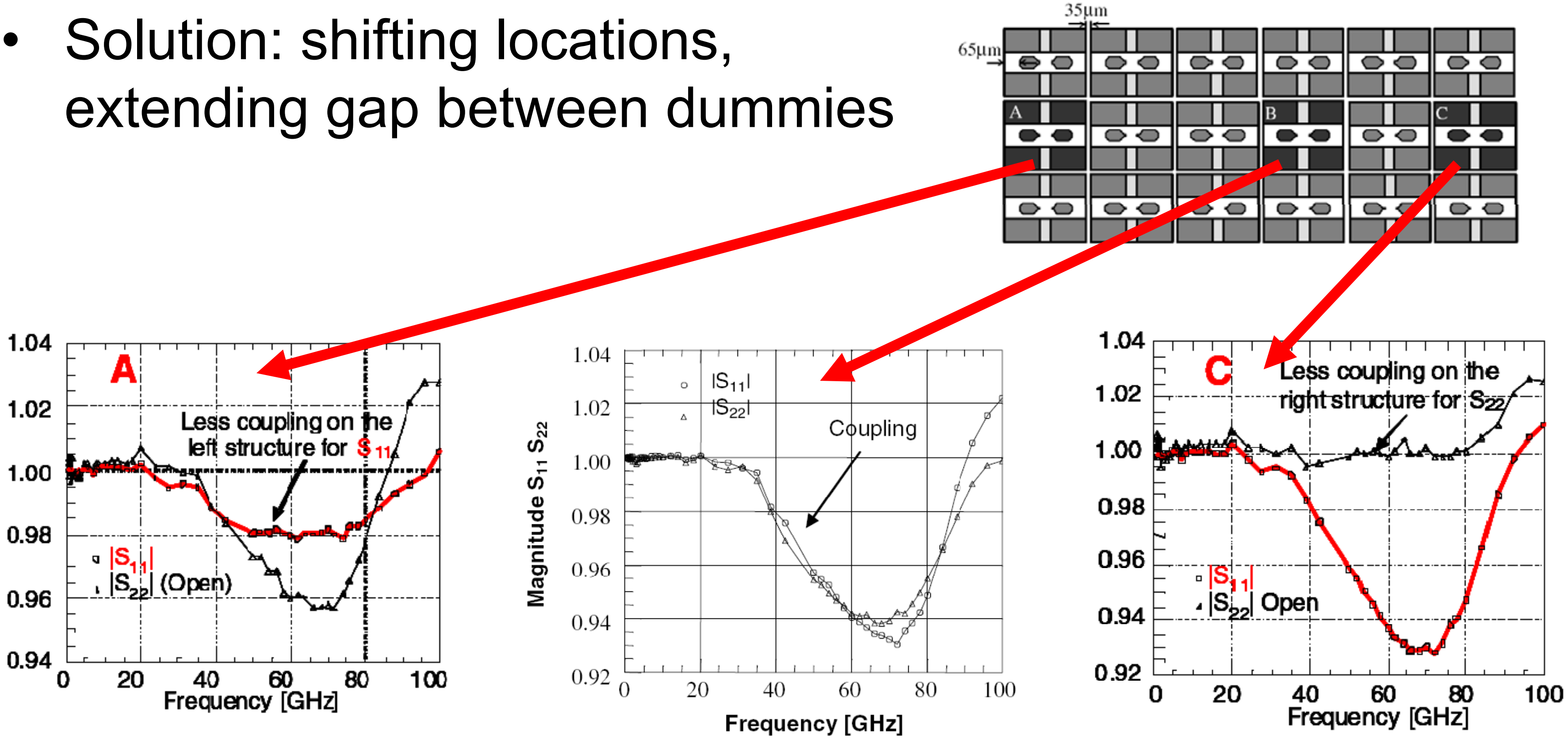


Q. Liang, J. D. Cressler, G. Niu, Y. Lu, G. Freeman, D. C. Ahlgren, R. M. Malladi, K. Newton, and D. L. Harame, "A simple four-port parasitic deembedding methodology for high-frequency scattering parameter and noise characterization of SiGe HBTs," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 51, pp. 2165-2174, 2003.

L. F. Tiemeijer, R. M. T. Pijper, J. A. van Steenwijk, and E. van der Heijden, "A New 12-Term Open-Short-Load de-embedding method for accurate on-wafer characterization of RF MOSFET structures," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 58, pp. 419-433, 2010.

Coupling Between Structures

- Problem: Open dummy
- Solution: shifting locations, extending gap between dummies

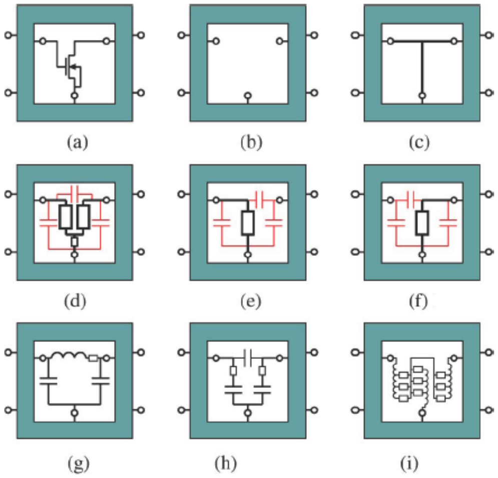


J. Bazzi, C. Raya, A. Curutchet, and T. Zimmer, "Investigation of high frequency coupling between probe tips and wafer surface," in *Bipolar/BiCMOS Circuits and Technology Meeting, 2009. BCTM 2009. IEEE*, 2009, pp. 87-90.

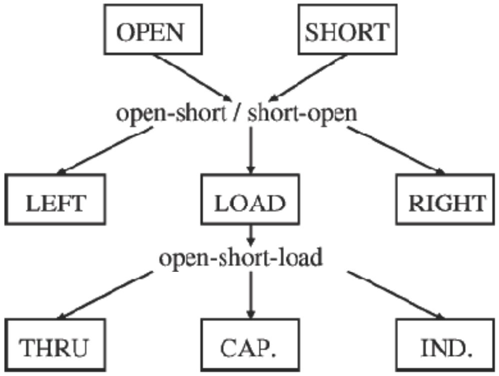
General Four-Port De-Embedding

- Problem: non-ideal standards (e.g. Short, Load)
- Solution: multi-step standard characterization method, based on the two-step de-embedding at low frequencies

Standard Parasitics



Standard Characterization Steps


OPEN
SHORT
open-short / short-open
LEFT
LOAD
RIGHT
open-short-load
THRU
CAP.
IND.

L. F. Tiemeijer, R. M. T. Pijper, J. A. van Steenwijk, and E. van der Heijden, "A New 12-Term Open-Short-Load de-embedding method for accurate on-wafer characterization of RF MOSFET structures," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 58, pp. 419-433, 2010.

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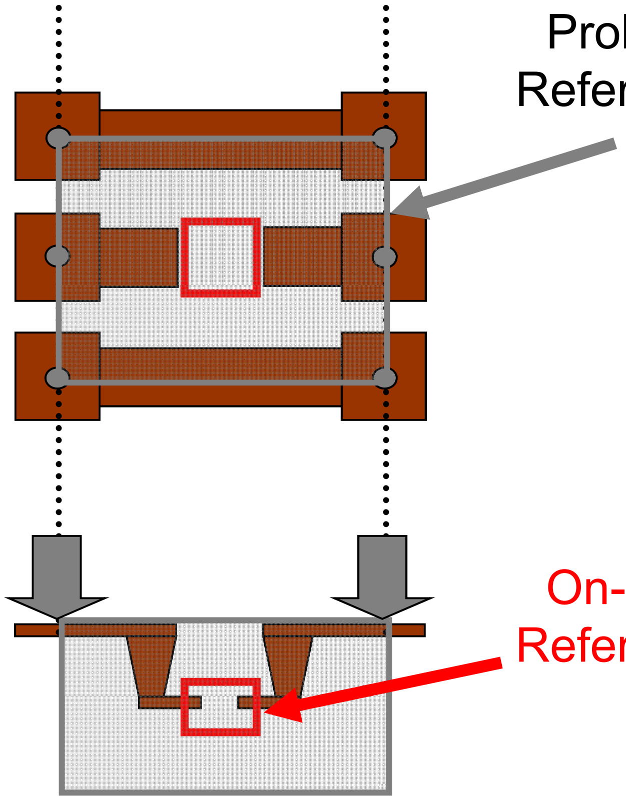
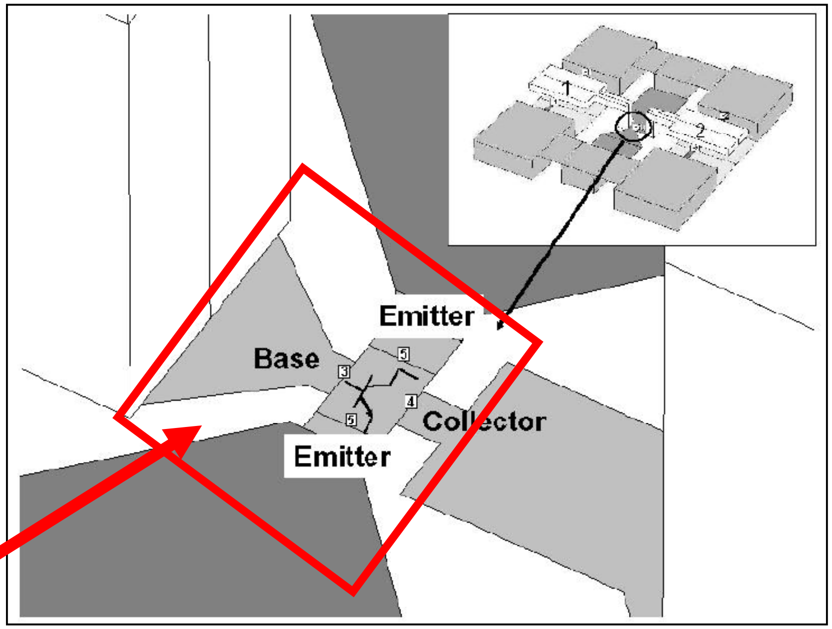
On-Wafer Calibration Goal

- To move the measurement reference plane close to the DUT terminals in just one step



Probe Tip Cal Reference plane

On-Wafer Cal Reference plane



Picture: R. Groves, BCTM, 2006

Suitable Calibration Methods

- Multiline TRL:
  - – Developed at NIST in early 90s
  - – Original application: semi-insulating wafers (GaAs)
  - – End of 90s: application techniques for Si
- LRM+:
  - – First application: SiGe:C
  - – Comparison vs. multiline TRL: GaAs, bulk Si

On-Wafer mTRL Calibration

Standards	Requirements / Conditions	Unknown	Self-Calibration Product
THRU	Known: S_{11}, S_{21}, S_{12}, S_{22}	---	---
LINE	Known: S_{11}, S_{22}; length	S_{21}, S_{12},	Propagation constant
REFLECT	$S_{11}=S_{22}$ $S_{11}(S_{22})$ known within +/- 90 degree	S_{11} (S_{22})	S_{11} (S_{22})

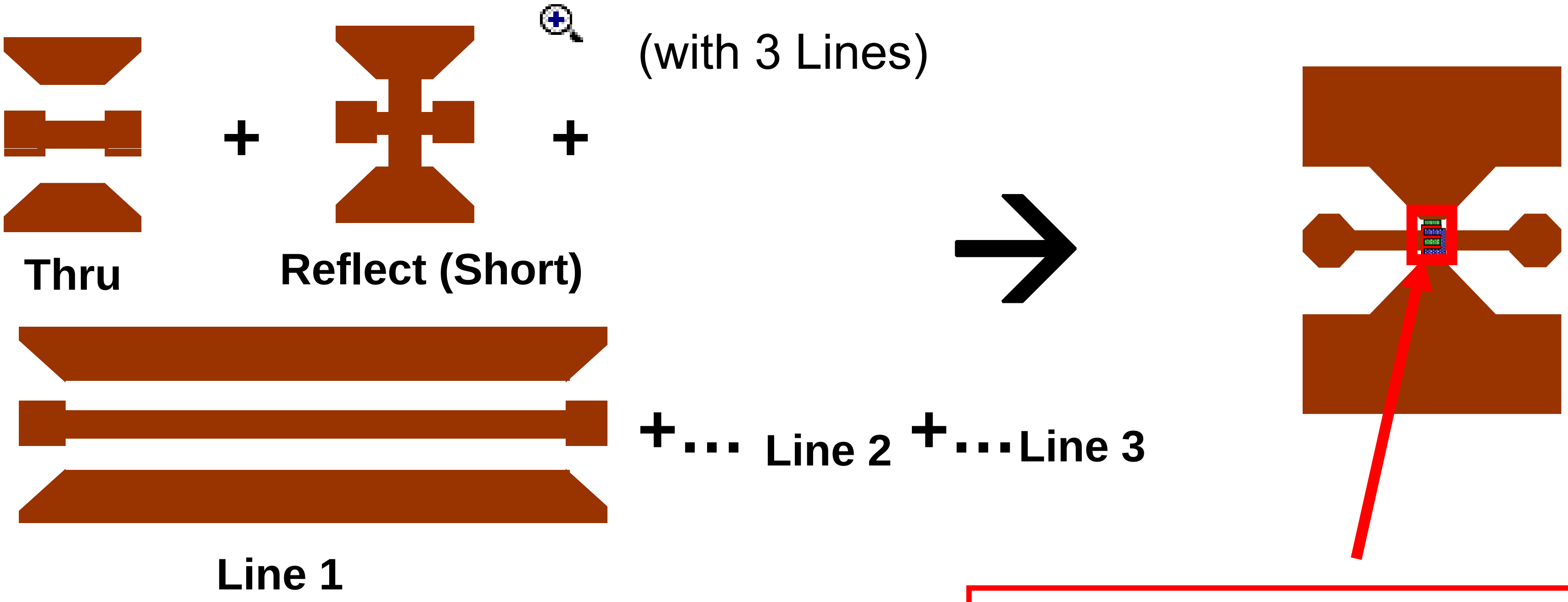
G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: an improved technique for calibrating the dual six-port automatic network analyzer," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 27, pp. 987-993, 1979.

R. B. Marks, "A multiline method of network analyzer calibration," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 39, pp. 1205-1215, 1991.

On-Wafer mTRL Calibration

- Advantages
  - Broadband
  - Does not require ideal Open or Short
  - Self-consistent
- Drawbacks
  - Many lines required
  - Characterization of Line Z_0
  - Sensitive to Reflect asymmetry

On-Wafer mTRL Calibration



(with 3 Lines)

Thru + **Reflect (Short)** +

Line 1 +… **Line 2** +…**Line 3**

Measurement reference plane after the on-wafer calibration

On-Wafer LRM+ Calibration

Standards	Requirements/ Conditions	Unknown	Self-Calibration Product
LINE **(Thru)**	Known: S_{11}, S_{21}, S_{12}, S_{22}	---	---
MATCH **(Load)**	Known: S_{11}, S_{22} $S_{11} \neq S_{22}$ Arbitrary impedance	---	---
REFLECT	$S_{11}=S_{22}$ $S_{11}(S_{22})$ known within +/- 90 degree	S_{11} (S_{22})	S_{11} (S_{22})

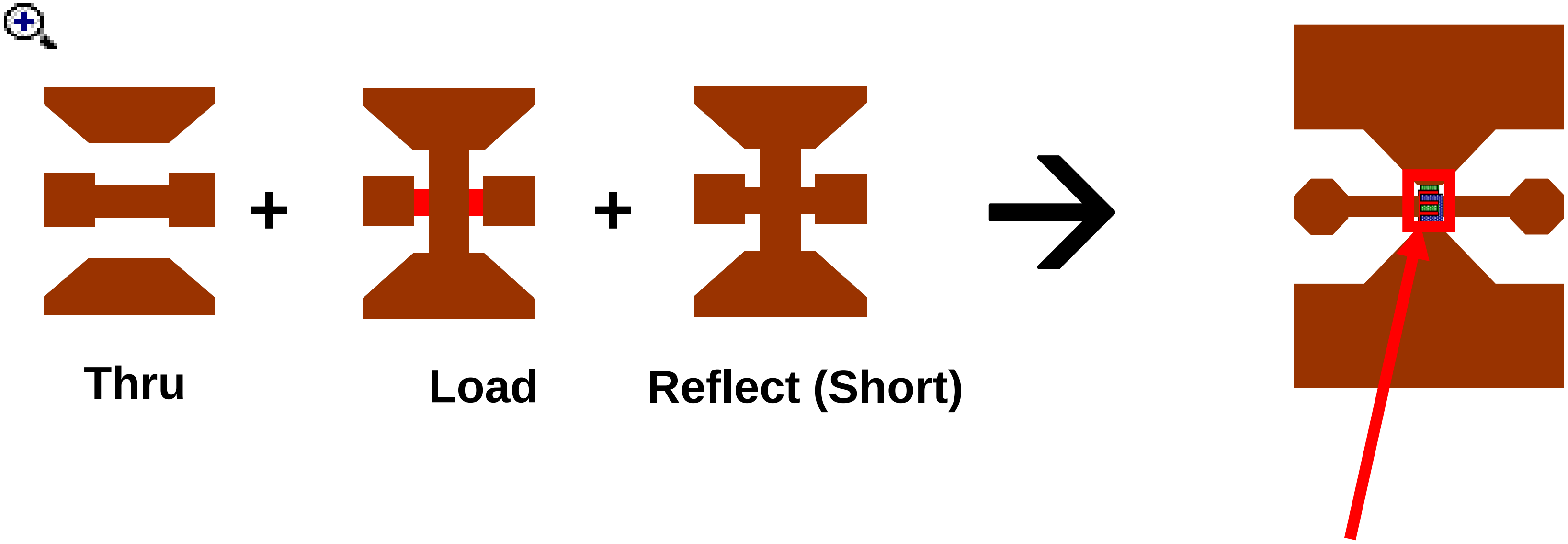
R. F. Scholz, F. Korndorfer, B. Senapati, and A. Rumiantsev, "Advanced technique for broadband on-wafer RF device characterization," in *ARFTG Microwave Measurements Conference-Spring, 63rd*, 2004, pp. 83-90.

On-Wafer LRM+ Calibration

- Advantages
  - Not sensitive to Load asymmetry
  - Arbitrary impedance elements can be used as Loads
  - Does not require known Open or Short
  - Self-consistent
- Drawbacks
  - Requires known Loads
  - Sensitive to Reflect asymmetry

On-Wafer LRM+ Calibration

- Example: LRM+ with wafer embedded (on-chip) standards



Measurement reference plane after the on-wafer calibration

Multiline TRL Case

Characterizing line Z_0

- 2D/3D EM simulation, but:
  - Complex cross-section model
  - Fabrication tolerances
- Lumped Load method, but:
  - Load impedance (resistance) must be known
- Calibration Comparison method, but:
  - Requires reference calibration

Lumped Load Method

- Multiline TRL calibration with reference impedance:

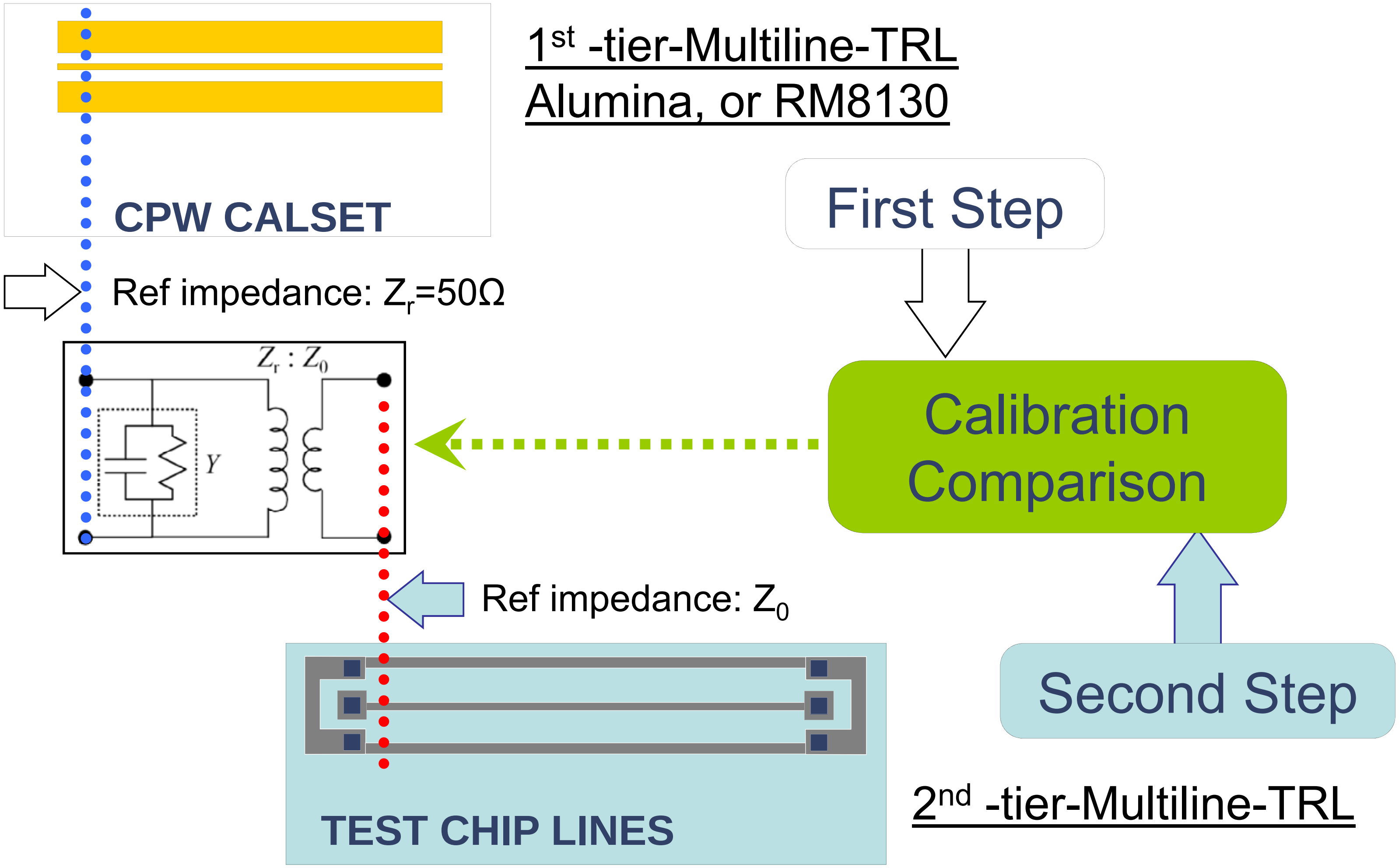
  $Z_r = Z_{line}$

- Measurement of Γ_{load} and $R_{load.dc}$ for the reference load
- Line capacitance is calculated from:

$$C\left[1 - j\frac{G}{\omega C}\right] \approx \frac{\gamma}{j\omega R_{load.dc}} \frac{1 + \Gamma_{load}}{1 - \Gamma_{load}}$$

D. F. Williams and R. B. Marks, "Transmission line capacitance measurement," *Microwave and Guided Wave Letters, IEEE,* vol. 1, pp. 243-245, 1991.

Calibration Comparison Method



1st -tier-Multiline-TRL
Alumina, or RM8130

CPW CALSET

First Step

Ref impedance: Z_r=50Ω

Calibration Comparison

Ref impedance: Z_0

Second Step

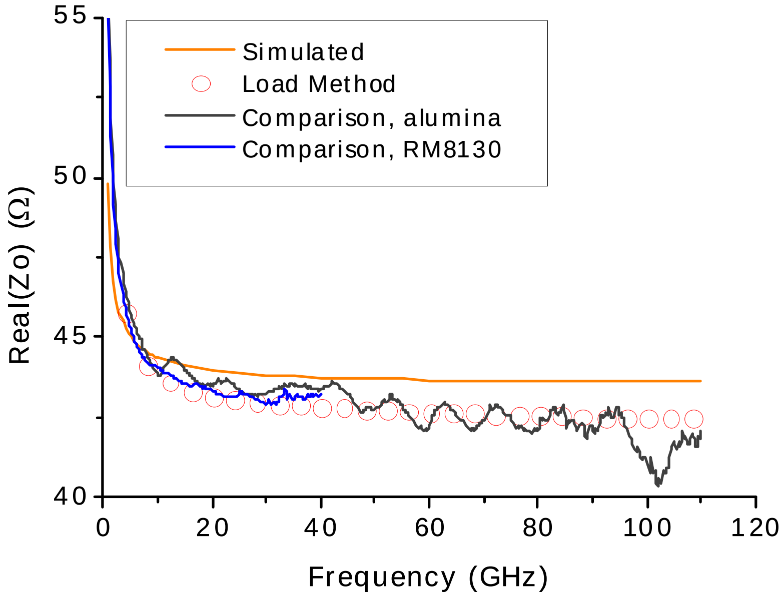
TEST CHIP LINES

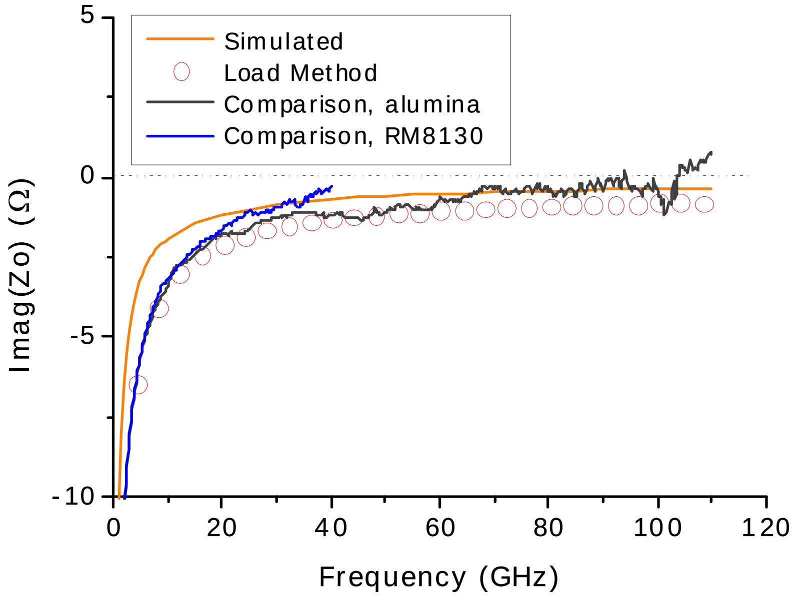
2nd -tier-Multiline-TRL

D. F. Williams, U. Arz, and H. Grabinski, "Characteristic-impedance measurement error on lossy substrates," *Microwave and Wireless Components Letters, IEEE,* vol. 11, pp. 299-301, 2001

Results Comparison

- Measurement of the line Z_0 on bulk silicon





All methods provided reliable results

A. Rumiantsev, P. L. Corson, S. L. Sweeney, and U. Arz, "Applying the calibration comparison technique for verification of transmission line standards on silicon up to 110 GHz," in *ARFTG Microwave Measurements Conference-Spring*, 73rd Boston, MA, 2009.

LRM+ Case

Load Impedance Z_{load} on Si

- 2D/3D EM simulation, but:
  - Complex cross-section model
  - Fabrication tolerances
- Referenced to NIST multiline TRL*, but:
  - Reference calibration required
- ‘Mixed Technique’**, but:
  - Requires measurement of the load resistance R_{load}

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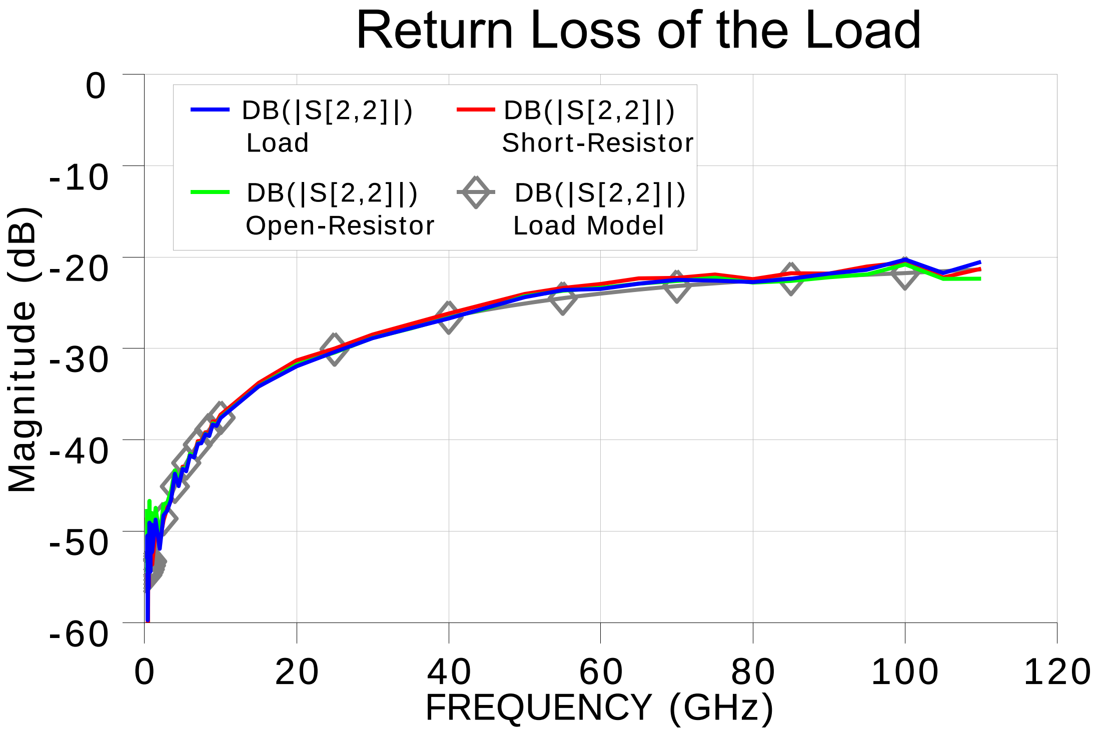
* A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," *ARFTG Microwave Measurements Conference-Fall*, 72nd, pp. 132-135, 2008.

** R. F. Scholz, F. Korndorfer, B. Senapati, and A. Rumiantsev, "Advanced technique for broadband on-wafer RF device characterization," in *ARFTG Microwave Measurements Conference-Spring, 63rd*, 2004, pp. 83-90.

Load Impedance Z_{LOAD}

- Fabrication tolerances within one test chip (mixed model vs. measurement)



Mixed model agrees with measurement results

A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," *ARFTG Microwave Measurements Conference-Fall*, 72nd, pp. 132-135, 2008.

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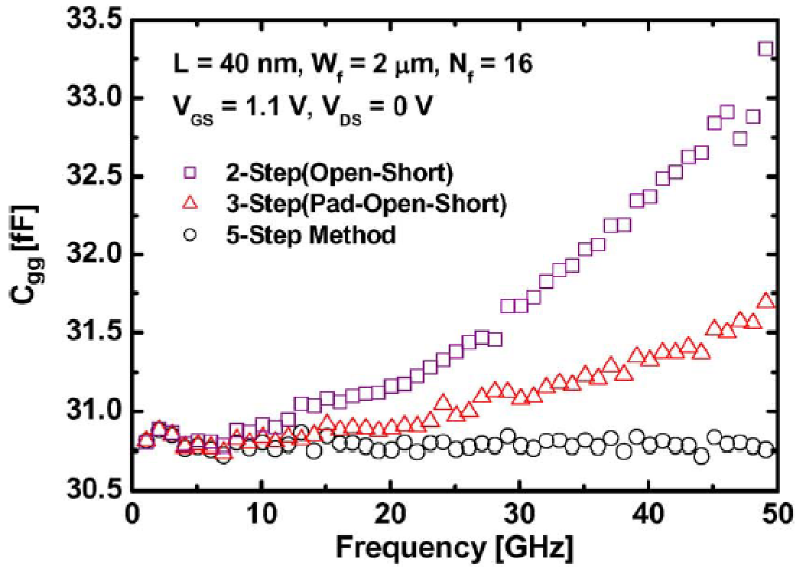
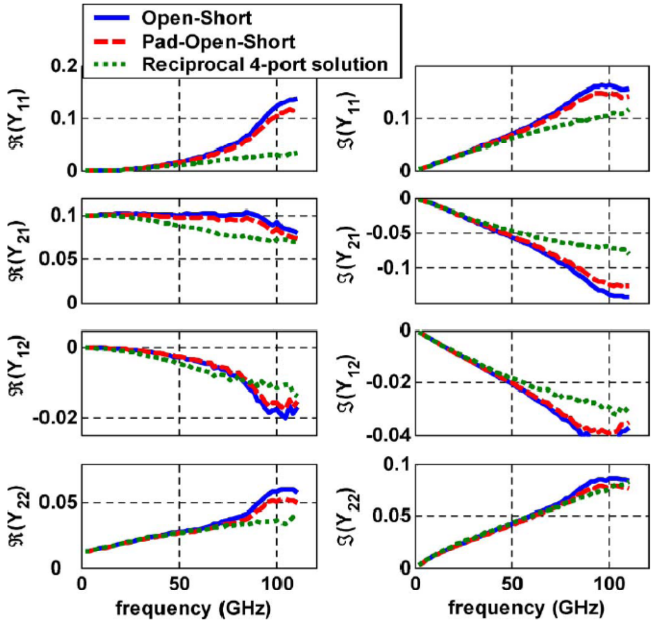
De-Embedding Comparison

- Difficult to compare all methods to each other
- Most publications present results below 50GHz



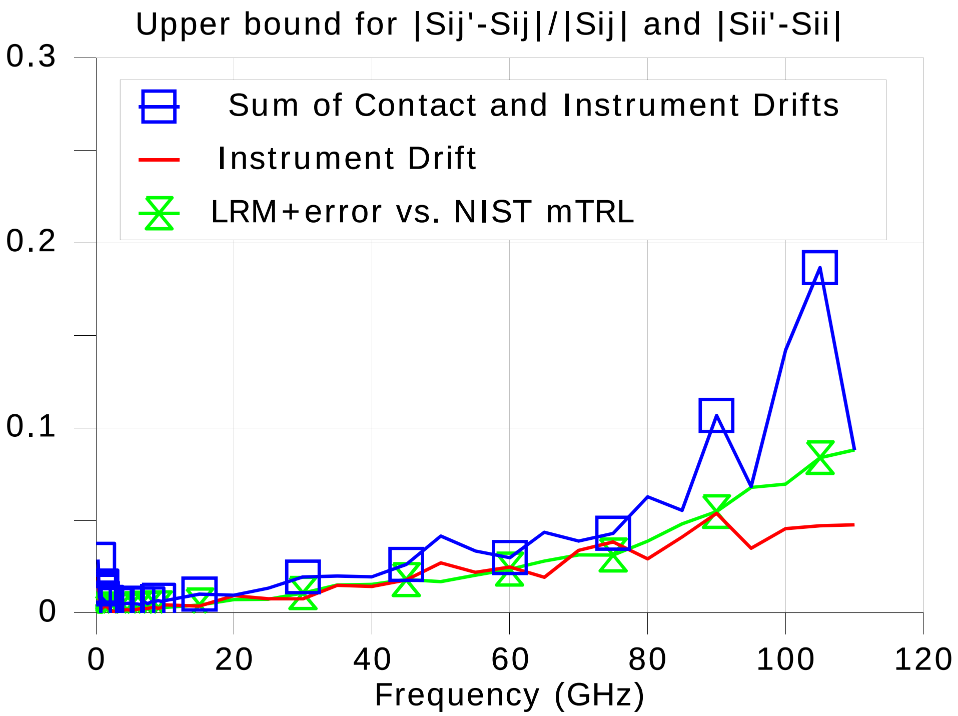


I. M. Kang, S.-J. Jung, T.-H. Choi, J.-H. Jung, C. Chung, H.-S. Kim, H. Oh, H. W. Lee, G. Jo, Y.-K. Kim, H.-G. Kim, and K.-M. Choi, "Five-step (Pad-Pad Short-Pad Open-Short-Open) de-embedding method and its verification," *Electron Device Letters, IEEE,* vol. 30, pp. 398-400, 2009.

X. Wei, G. Niu, S. Sweeney, Q. Liang, X. Wang, and S. Taylor, "A general 4-port solution for 110 GHz on-wafer transistor measurements with or without impedance standard substrate (ISS) calibration," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 2706-2714, 2007.

LRM+ and mTRL Comparison

- Comparison of different calibration schemes on Si

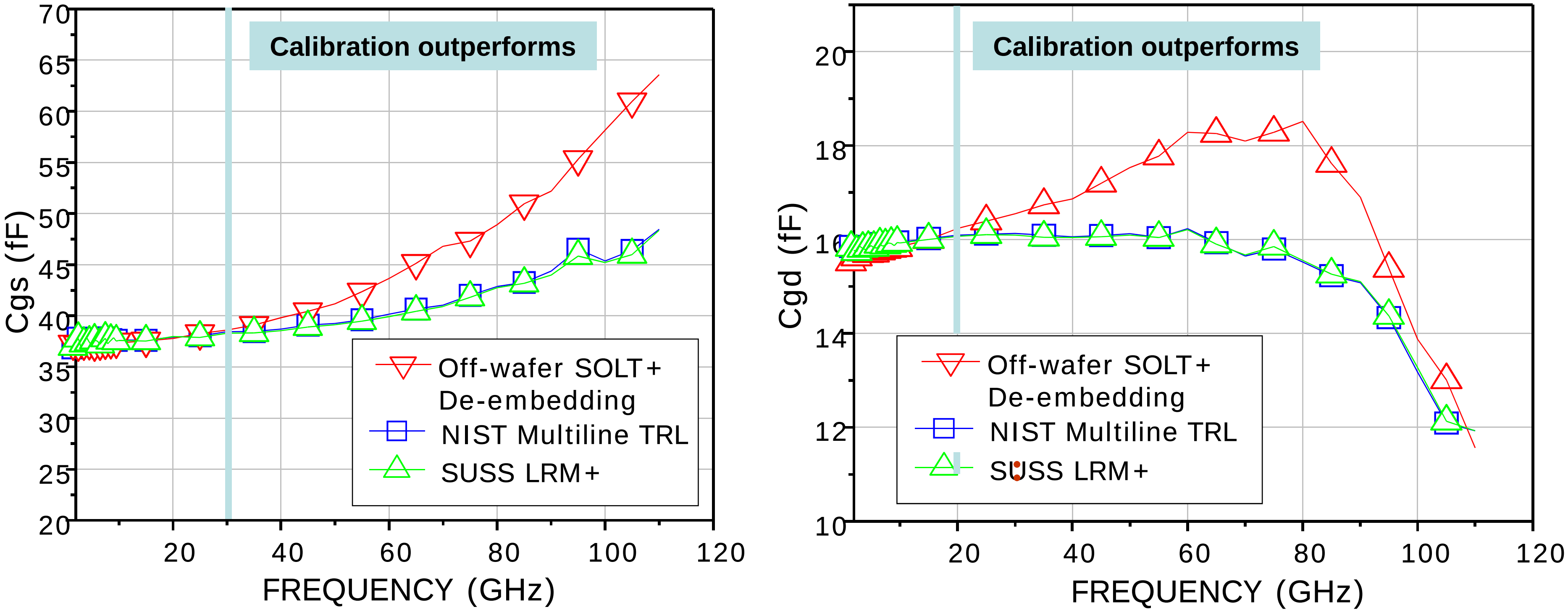


A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," *ARFTG Microwave Measurements Conference-Fall*, 72nd, pp. 132-135, 2008.

- LRM+ is in agreement with the reference mTRL

On-Wafer Calibration vs. De-Embedding Comparison

- Verification on advanced 0.13 µm RF-CMOS NFET



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Conclusion

- Different contact pad de-embedding routines and calibration methods are available today
- Decrease in accuracy, increase in complexity of contact pads de-embedding approach with the measurement frequency
- On-wafer calibration enables setting the measurement reference plane close to the transistor terminals

Conclusion (Cont.)

Advantages of the On-Wafer Calibration:

- Improved measurement accuracy at mm-wave frequencies
- Reduced test chip size for LRM+
- Self-consistent → easy to check for errors
- Open not required → reduced influence of coupling problems